M2 Integration Circuits Systems

EA2 - Année Scolaire 2016-2017(S1)

Exam

Durée 1h30 - Authorized documents and calculator

Exercices

Exercice Low power radio receiver **2**

Exercice Frequency Synthesis **3**

Exercice Transmitter and Receiver Switch **3**

Tous les exercices sont indépendants.

Direction de la Formation Initiale
Département Communications et Électronique
École Nationale Supérieure des Télécommunications

Exercice 1 - Low power radio receiver

We are interested in low power communications in the 2.4GHz band. In this standard a useful channel occupies a band of 1MHz. Its sensitivity at the antenna is -70 dBm. In order to correctly decode the signal in the baseband digital part, this receiver must guarantee at the output a minimum signal-to-noise ratio SNRmin = 21 dB. From these data find :

Question 1.1 The level of the thermal noise floor at ambient temperature, in the channel at the receiving antenna.

Question 1.2 The maximum Noise Figure (NF) that the receiver could have while ensuring an output SNR greater than SNRmin.

The diagram below shows the architecture of the chosen receiver. It is assumed that the RF filter does not change the signal level, nor the noise level.

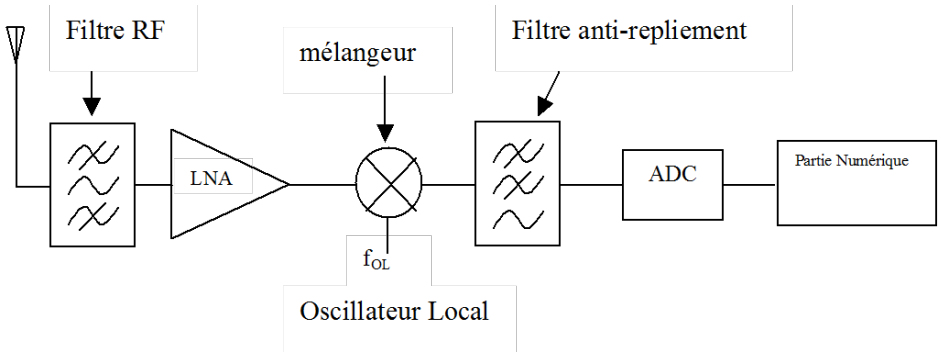

FIGURE 1 – Low power radio receiver

TABLE 1 – Gain et NF

	Gain(dB)	NF(dB)
LNA	20	3
Mixer	10	12

The table above gives the gain and Noise Figure values of the LNA and the mixer

Question 1.3 Calculate the signal power at the output of the LNA and the noise figure between the input of the chain and the output of the LNA. Deduce the maximum noise figure that could be allowed between the output of the LNA and the output of the receiver while guaranteeing the SNRmin at output.

Question 1.4 Do the same at the mixer output.

Question 1.5 Assume that the signals dynamic range (ratio between the max signal and the min signal) is 40 dB at the input of the analog-digital converter (ADC) and that SNRmin = 21 dB is respected at the input of the ADC. If the quantization noise level is placed 10 dB below the thermal noise floor, calculate the minimum resolution of the converter in number of bits. (For this calculation, you can assume that the input signal is a sinusoid).

Exercice 2 - Frequency Synthesis

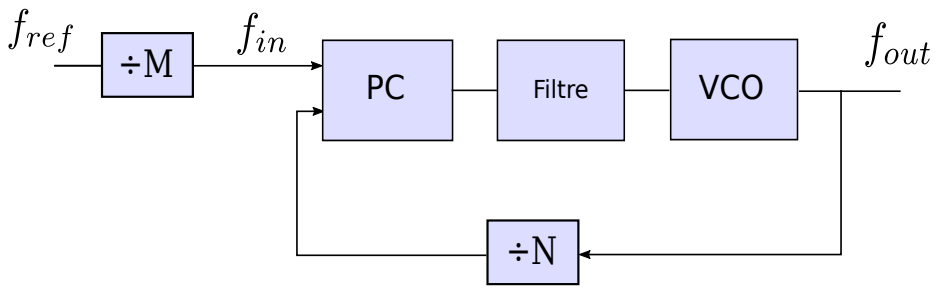

FIGURE 2 – Phase Locked Loop (PLL)

A phase locked loop is used for the local oscillator of a Bluetooth receiver (figure 2) with an integer frequency divider N in the feedback loop and an integer divider M on the reference frequency f_{ref}. Since the frequency conversion is direct (FI = 0), the central frequencies of the 79 channels of the system :

$$f_k = (2402 + k)\ MHz, \qquad k = 0, ..., 78$$

The reference frequency is obtained from a quartz oscillator with $f_{ref} = 10\ MHz$.

Question 2.1 Determine the value of the division factor M. Deduce the value of the division factor N in function of the channel k.

Question 2.2 What is the impact of the division factor N on the phase noise L_r of the quartz reference source in the PLL bandwidth ?

Exercice 3 - Transmitter and Receiver Switch

This switch consists of AsGa MESFET transistors with grid length of 0.8 μm. At the frequency of 1.9 GHz, the insulations are 29-35dB and the insertion losses are 0.9-1.5 dB.

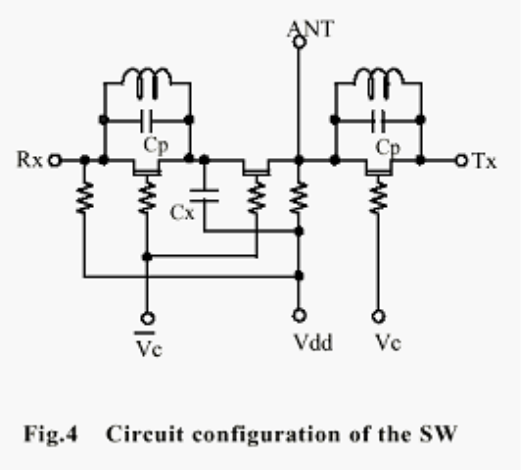

Fig.4 Circuit configuration of the SW

Question 3.1 Explain the operation of this duplexer.

Question 3.2 What is its function in an RF transmitter and receiver ?

Question 3.3 Why use AsGa ?

Question 3.4 Why use the L, Cp elements ?

Question 3.5 In your opinion,what is the size (grid development) of the MesFet ?

Question 3.6 Why do we get different values of insulation and losses ?