24-Bit, 312 kSPS, 109 dB Sigma-Delta ADC with On-Chip Buffers and Serial Interface

AD7764

FEATURES

High performance 24-bit Σ-Δ ADC
115 dB dynamic range at 78 kHz output data rate
109 dB dynamic range at 312 kHz output data rate
312 kHz maximum fully filtered output word rate
Pin-selectable oversampling rate (64×, 128×, and 256×)
Low power mode
Flexible SPI
Fully differential modulator input
On-chip differential amplifier for signal buffering
On-chip reference buffer
Full band low-pass finite impulse response (FIR) filter
Overrange alert pin
Digital gain correction registers
Power-down mode
Synchronization of multiple devices via $\overline{\text{SYNC}}$ pin
Daisy chaining

APPLICATIONS

Data acquisition systems
Vibration analysis
Instrumentation

FUNCTIONAL BLOCK DIAGRAM

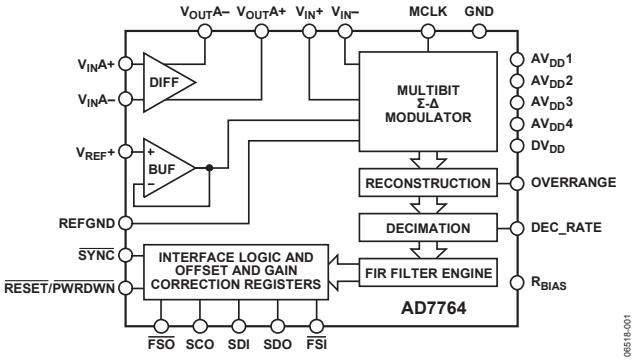

Figure 1.

Table 1. Related Devices

Part No.	Description
AD7760	2.5 MSPS, 100 dB, parallel output on-chip buffers
AD7762	625 kSPS, 109 dB, parallel output on-chip buffers
AD7763	625 kSPS, 109 dB, serial output, on-chip buffers
AD7765	156 kSPS, 112 dB, serial output, on-chip buffers
AD7766	128/64/32 kSPS, 8.5 mW, 109 dB SNR
AD7767	128/64/32 kSPS, 8.5 mW, 109 dB SNR

GENERAL DESCRIPTION

The AD7764 is a high performance, 24-bit sigma-delta (Σ-Δ) analog-to-digital converter (ADC). It combines wide input bandwidth, high speed, and performance of 109 dB dynamic range at a 312 kHz output data rate. With excellent dc specifications, the converter is ideal for high speed data acquisition of ac signals where dc data is also required.

Using the AD7764 eases the front-end antialias filtering requirements, simplifying the design process significantly. The AD7764 offers pin-selectable decimation rates of 64×, 128×, and 256×. Other features include an integrated buffer to drive the reference, as well as a fully differential amplifier to buffer and level shift the input to the modulator.

An overrange alert pin indicates when an input signal has exceeded the acceptable range. The addition of internal gain and internal overrange registers makes the AD7764 a compact, highly integrated data acquisition device requiring minimal peripheral components.

The AD7764 also offers a low power mode, significantly reducing power dissipation without reducing the output data rate or available input bandwidth.

The differential input is sampled at up to 40 MSPS by an analog modulator. The modulator output is processed by a series of low-pass filters. The external clock frequency applied to the AD7764 determines the sample rate, filter corner frequencies, and output word rate.

The AD7764 device boasts a full band on-board FIR filter. The full stop-band attenuation of the filter is achieved at the Nyquist frequency. This feature offers increased protection from signals that lie above the Nyquist frequency being aliased back into the input signal bandwidth.

The reference voltage supplied to the AD7764 determines the input range. With a 4 V reference, the analog input range is ±3.2768 V differential, biased around a common mode of 2.048 V. This common-mode biasing can be achieved using the on-chip differential amplifier, further reducing the external signal conditioning requirements.

The AD7764 is available in a 28-lead TSSOP package and is specified over the industrial temperature range of −40°C to +85°C.

Rev. A

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6/07—Revision 0: Initial Version

SPECIFICATIONS

$AV_{DD}1 = DV_{DD} = 2.5$ V, $AV_{DD}2 = AV_{DD}3 = AV_{DD}4 = 5$ V, $V_{REF}+ = 4.096$ V, MCLK amplitude = 5 V, $T_A = 25°C$, normal power mode, using the on-chip amplifier with components, as shown in the Optimal row in Table 7, unless otherwise noted.[1]

Table 2.

Parameter	Test Conditions/Comments	Specification	Unit
DYNAMIC PERFORMANCE			
Decimate 256×			
Normal Power Mode	MCLK = 40 MHz, ODR = 78.125 kHz, f_{IN} = 1 kHz sine wave		
Dynamic Range	Modulator inputs shorted	115	dB typ
		110	dB min
	Differential amplifier inputs shorted	113.4	dB typ
Signal-to-Noise Ratio (SNR)[2]	Input amplitude = −0.5 dB	109	dB typ
		106	dB min
Spurious-Free Dynamic Range (SFDR)	Nonharmonic	130	dBFS typ
Total Harmonic Distortion (THD)	Input amplitude = −0.5 dB	−105	dB typ
	Input amplitude = −6 dB	−103	dB typ
	Input amplitude = −60 dB	−71	dB typ
Low Power Mode	MCLK = 40 MHz, ODR = 78.125 kHz, f_{IN} = 1 kHz sine wave		
Dynamic Range	Modulator inputs shorted	113	dB typ
		110	dB min
	Differential amplifier inputs shorted	112	dB typ
Signal-to-Noise Ratio (SNR)[2]	Input amplitude = −0.5 dB	109	dB typ
		106	dB min
Total Harmonic Distortion (THD)	Input amplitude = −0.5 dB	−105	dB typ
	Input amplitude = −6 dB	−111	dB typ
	Input amplitude = −6 dB	−100	dB max
	Input amplitude = −60 dB	−76	dB typ
Decimate 128×			
Normal Power Mode	MCLK = 40 MHz, ODR = 156.25 kHz, f_{IN} = 1 kHz sine wave		
Dynamic Range	Modulator inputs shorted	112	dB typ
		108	dB min
	Differential amplifier inputs shorted	110.4	dB typ
Signal-to-Noise Ratio (SNR)[2]		107	dB typ
		105	dB min
Spurious-Free Dynamic Range (SFDR)	Nonharmonic	130	dBFS typ
Total Harmonic Distortion (THD)	Input amplitude = −0.5 dB	−105	dB typ
	Input amplitude = −6 dB	−103	dB typ
Intermodulation Distortion (IMD)	Input amplitude = −6 dB, f_{IN} A = 50.3 kHz, f_{IN} B = 47.3 kHz		
	Second-order terms	−117	dB typ
	Third-order terms	−108	dB typ
Low Power Mode	MCLK = 40 MHz, ODR = 156.25 kHz, f_{IN} = 1 kHz sine wave		
Dynamic Range	Modulator inputs shorted	110	dB typ
		109	dB min
	Differential amplifier inputs shorted	109	dB typ
Signal-to-Noise Ratio (SNR)[2]	Input amplitude = −0.5 dB	107	dB typ
		105	dB min
Total Harmonic Distortion (THD)	Input amplitude = −0.5 dB	−105	dB typ
	Input amplitude = −6 dB	−111	dB typ
	Input amplitude = −6 dB	−100	dB max
Intermodulation Distortion (IMD)	Input amplitude = −6 dB, f_{IN} A = 50.3 kHz, f_{IN} B = 47.3 kHz		
	Second-order terms	−134	dB typ
	Third-order terms	−110	dB typ

Parameter	Test Conditions/Comments	Specification	Unit
Decimate 64×			
Normal Power Mode	MCLK = 40 MHz, ODR = 312.5 kHz, f_{IN} = 1 kHz sine wave		
Dynamic Range	Modulator inputs shorted	109	dB typ
		105	dB min
	Differential amplifier inputs shorted	107.3	dB typ
Signal-to-Noise Ratio (SNR)[2]		104	dB typ
		102.7	dB min
Spurious-Free Dynamic Range (SFDR)	Nonharmonic	130	dBFS typ
Total Harmonic Distortion (THD)	Input amplitude = −0.5 dB	−105	dB typ
	Input amplitude = −6 dB	−103	dB typ
Intermodulation Distortion (IMD)	Input amplitude = −6 dB, f_{IN} A = 100.3 kHz, f_{IN} B = 97.3 kHz		
	Second-order terms	−118	dB
	Third-order terms	−108	dB
Low Power Mode			
Dynamic Range	Modulator inputs shorted	106	dB typ
		105	dB min
	Differential amplifier inputs shorted	105.3	
Signal-to-Noise Ratio (SNR)[2]	Input amplitude = −0.5 dB	103	dB typ
		102	dB min
Spurious-Free Dynamic Range (SFDR)	Nonharmonic	110	dBFS typ
Total Harmonic Distortion (THD)	Input amplitude = −0.5 dB	−105	dB typ
	Input amplitude = −6 dB	−111	dB typ
		−100	dB max
DC ACCURACY			
Resolution	Guaranteed monotonic to 24 bits	24	Bits
Integral Nonlinearity	Normal power mode	0.0036	% typ
	Low power mode	0.0014	% typ
Zero Error	Normal power mode	0.006	% typ
		0.03	% max
	Including on-chip amplifier	0.04	% typ
	Low power mode	0.002	% typ
		0.024	% max
Gain Error		0.018	% typ
	Including on-chip amplifier	0.04	% typ
Zero Error Drift		0.00006	%FS/°C typ
Gain Error Drift		0.00005	%FS/°C typ
DIGITAL FILTER CHARACTERISTICS			
Pass-Band Ripple		0.1	dB typ
Pass Band[3]	−1 dB frequency	ODR × 0.4016	kHz
−3 dB Bandwidth[3]		ODR × 0.4096	kHz
Stop Band[3]	Beginning of stop band	ODR × 0.5	kHz
Stop-Band Attenuation	Decimate 64× and decimate 128× modes	−120	dB typ
	Decimate 256×	−115	dB typ
Group Delay			
Decimate 64×	MCLK = 40 MHz	89	µs typ
Decimate 128×	MCLK = 40 MHz	177	µs typ
Decimate 256×	MCLK = 40 MHz	358	µs typ
ANALOG INPUT			
Differential Input Voltage	Modulator input pins: $V_{IN}+ - V_{IN}-$, $V_{REF}+$ = 4.096 V	±3.2768	V p-p
Input Capacitance	At on-chip differential amplifier inputs	5	pF typ
	At modulator inputs	29	pF typ

Parameter	Test Conditions/Comments	Specification	Unit
REFERENCE INPUT/OUTPUT			
V_{REF+} Input Voltage	$AV_{DD}3 = 5\ V \pm 5\%$	4.096	V
V_{REF+} Input DC Leakage Current		±1	µA max
V_{REF+} Input Capacitance		5	pF typ
DIGITAL INPUT/OUTPUT			
MCLK Input Amplitude		2.25 to 5.25	V
Input Capacitance		7.3	pF typ
Input Leakage Current		±1	µA/pin max
V_{INH}		$0.8 \times DV_{DD}$	V min
V_{INL}		$0.2 \times DV_{DD}$	V max
V_{OH}[4]		2.2	V min
V_{OL}		0.1	V max
ON-CHIP DIFFERENTIAL AMPLIFIER			
Input Impedance		>1	MΩ
Bandwidth for 0.1 dB Flatness		125	kHz
Common-Mode Input Voltage	Voltage range at input pins: $V_{IN}A+$ and $V_{IN}A-$	−0.5 to +2.2	V
Common-Mode Output Voltage	On-chip differential amplifier pins: $V_{OUT}A+$ and $V_{OUT}A-$	2.048	V
POWER REQUIREMENTS			
$AV_{DD}1$ (Modulator Supply)	±5%	2.5	V
$AV_{DD}2$ (General Supply)	±5%	5	V
$AV_{DD}3$ (Differential Amplifier Supply)	±5%	5	V min/max
$AV_{DD}4$ (Ref Buffer Supply)	±5%	5	V min/max
DV_{DD}	±5%	2.5	V
Normal Power Mode			
$AI_{DD}1$ (Modulator)		19	mA typ
$AI_{DD}2$ (General)[5]	MCLK = 40 MHz	13	mA typ
$AI_{DD}3$ (Differential Amplifier)	$AV_{DD}3 = 5\ V$	10	mA typ
$AI_{DD}4$ (Reference Buffer)	$AV_{DD}4 = 5\ V$	9	mA typ
DI_{DD}[5]	MCLK = 40 MHz	37	mA typ
Low Power Mode			
$AI_{DD}1$ (Modulator)		10	mA typ
$AI_{DD}2$ (General)[5]	MCLK = 40 MHz	7	mA typ
$AI_{DD}3$ (Differential Amplifier)	$AV_{DD}3 = 5\ V$	5.5	mA typ
$AI_{DD}4$ (Reference Buffer)	$AV_{DD}4 = 5\ V$	5	mA typ
DI_{DD}[5]	MCLK = 40 MHz	20	mA typ
POWER DISSIPATION			
Normal Power Mode	MCLK = 40 MHz, decimate 64×	300	mW typ
		371	mW max
Low Power Mode	MCLK = 40 MHz, decimate 64×	160	mW typ
		215	mW max
Power-Down Mode[6]	$\overline{PWRDWN}$ held logic low	1	mW typ

[1] See the Terminology section.
[2] SNR specifications in decibels are referred to a full-scale input, FS. Tested with an input signal at 0.5 dB below full scale, unless otherwise specified.
[3] Output data rate (ODR) = [(MCLK/2)]/decimation rate. That is, the maximum ODR for AD7764 = [(40 MHz)/2)/64] = 312.5 kHz.
[4] Tested with a 400 µA load current.
[5] Tested at MCLK = 40 MHz. This current scales linearly with the MCLK frequency applied.
[6] Tested at 125°C.

TIMING SPECIFICATIONS

$AV_{DD}1 = DV_{DD} = 2.5$ V, $AV_{DD}2 = AV_{DD}3 = AV_{DD}4 = 5$ V, $V_{REF}+ = 4.096$ V, $T_A = 25°C$, $C_{LOAD} = 25$ pF.

Table 3.

Parameter	Limit at T_{MIN}, T_{MAX}	Unit	Description
f_{MCLK}	500	kHz min	Applied master clock frequency
	40	MHz max	
f_{ICLK}	250	kHz min	Internal modulator clock derived from MCLK
	20	MHz max	
t_1	$1 \times t_{ICLK}$	typ	SCO high period
t_2	$1 \times t_{ICLK}$	typ	SCO low period
t_3	1	ns typ	SCO rising edge to $\overline{FSO}$ falling edge
t_4	2	ns typ	Data access time, $\overline{FSO}$ falling edge to data active
t_5	8	ns max	MSB data access time, SDO active to SDO valid
t_6	40	ns min	Data hold time (SDO valid to SCO rising edge)
t_7	9.5	ns max	Data access time (SCO rising edge to SDO valid)
t_8	2	ns typ	SCO rising edge to $\overline{FSO}$ rising edge
t_9	$32 \times t_{SCO}$	max	$\overline{FSO}$ low period
t_{10}	12	ns min	Setup time from $\overline{FSI}$ falling edge to SCO falling edge
t_{11}	$1 \times t_{SCO}$	min	$\overline{FSI}$ low period
t_{12}[1]	$32 \times t_{SCO}$	max	$\overline{FSI}$ low period
t_{13}	12	ns min	SDI setup time for the first data bit
t_{14}	12	ns min	SDI setup time
t_{15}	0	ns max	SDI hold time
$t_{R\ MIN}$	$1 \times t_{MCLK}$	min	Minimum time for a valid $\overline{RESET}$ pulse
$t_{R\ HOLD}$	5	ns min	Minimum time between the MCLK rising edge and $\overline{RESET}$ rising edge
$t_{R\ SETUP}$	5	ns min	Minimum time between the $\overline{RESET}$ rising edge and MCLK rising edge
$t_{S\ MIN}$	$4 \times t_{MCLK}$	min	Minimum time for a valid $\overline{SYNC}$ pulse
$t_{S\ HOLD}$	5	ns min	Minimum time between the MCLK falling edge and $\overline{SYNC}$ rising edge
$t_{S\ SETUP}$	5	ns min	Minimum time between the $\overline{SYNC}$ rising edge and MCLK falling edge

[1] This is the maximum time $\overline{FSI}$ can be held low when writing to an individual device (a device that is not daisy-chained).

TIMING DIAGRAMS

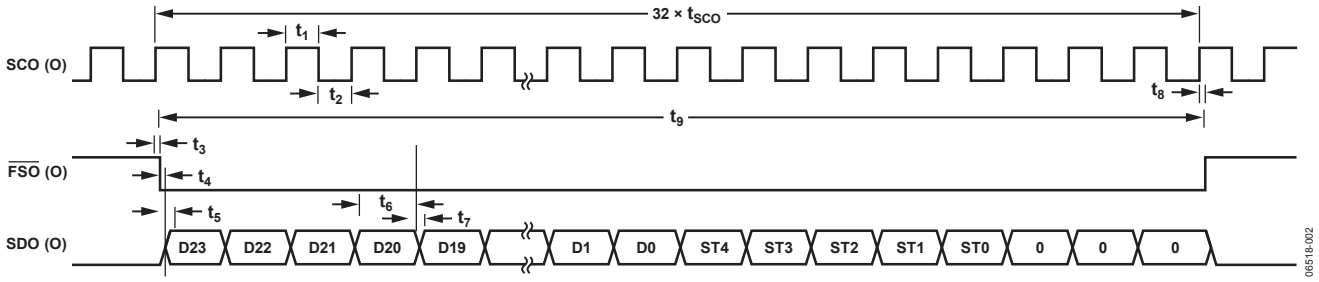

Figure 2. Serial Read Timing Diagram

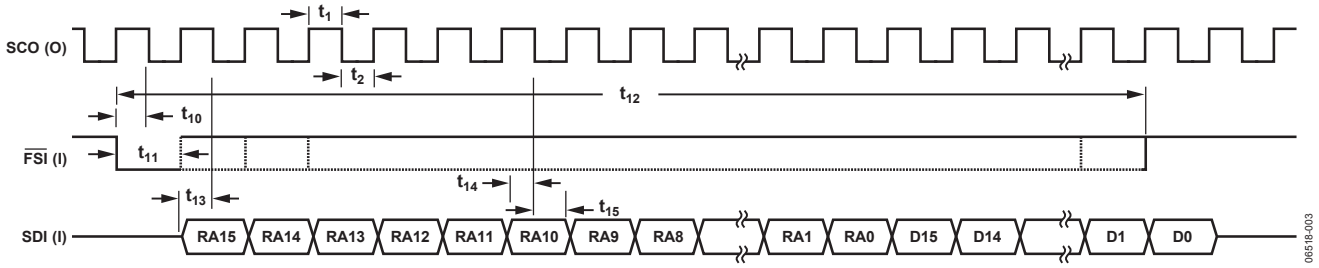

Figure 3. AD7764 Register Write

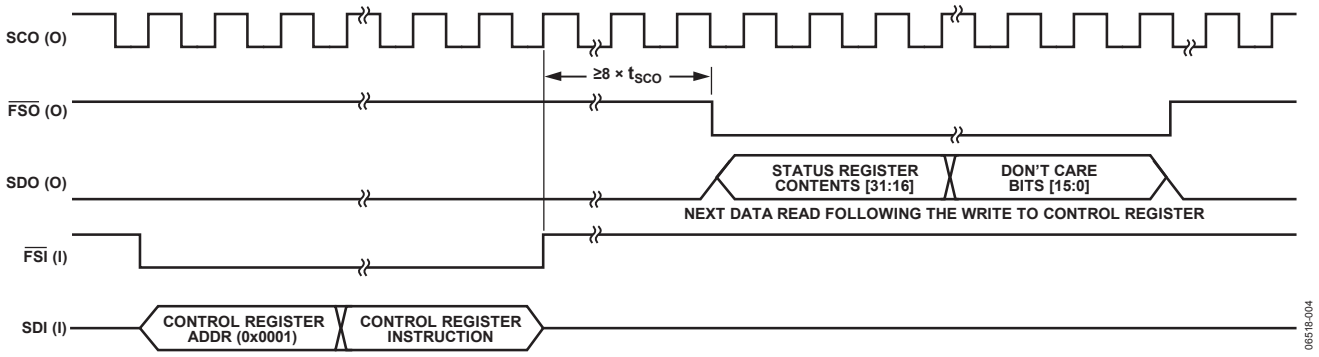

Figure 4. AD7764 Status Register Read Cycle

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 4.

Parameter	Rating
$AV_{DD}1$ to GND	−0.3 V to +2.8 V
$AV_{DD}2$, $AV_{DD}3$, $AV_{DD}4$ to GND	−0.3 V to +6 V
DV_{DD} to GND	−0.3 V to +2.8 V
$V_{IN}A+$, $V_{IN}A-$ to GND[1]	−0.3 V to +6 V
$V_{IN}+$, $V_{IN}-$ to GND[1]	−0.3 V to +6 V
Digital Input Voltage to GND[2]	−0.3 V to +2.8 V
$V_{REF}+$ to GND[3]	−0.3 V to +6 V
Input Current to Any Pin Except Supplies[4]	±10 mA
Operating Temperature Range	
Commercial	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
TSSOP Package	
θ_{JA} Thermal Impedance	143°C/W
θ_{JC} Thermal Impedance	45°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C
ESD	1 kV

[1] Absolute maximum voltage for $V_{IN}-$, $V_{IN}+$, $V_{IN}A-$, and $V_{IN}A+$ is 6.0 V or $AV_{DD}3$ + 0.3 V, whichever is lower.
[2] Absolute maximum voltage on digital input is 3.0 V or DV_{DD} + 0.3 V, whichever is lower.
[3] Absolute maximum voltage on $V_{REF}+$ input is 6.0 V or $AV_{DD}4$ + 0.3 V, whichever is lower.
[4] Transient currents of up to 100 mA do not cause SCR latch-up.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

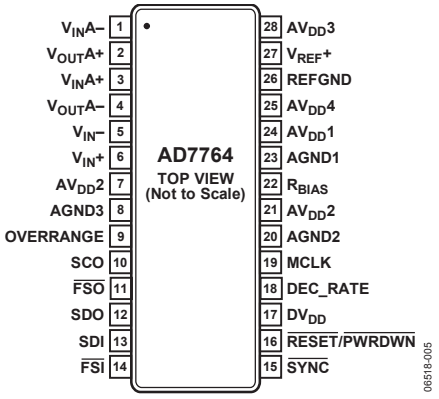

Figure 5. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
24	$AV_{DD}1$	2.5 V Power Supply for Modulator. This pin should be decoupled to AGND1 (Pin 23) with a 100 nF capacitor.
7 and 21	$AV_{DD}2$	5 V Power Supply. Pin 7 should be decoupled to AGND3 (Pin 8) with a 100 nF capacitor. Pin 21 should be decoupled to AGND1 (Pin 23) with a 100 nF capacitor.
28	$AV_{DD}3$	3.3 V to 5 V Power Supply for Differential Amplifier. This pin should be decoupled to the ground plane with a 100 nF capacitor.
25	$AV_{DD}4$	3.3 V to 5 V Power Supply for Reference Buffer. This pin should be decoupled to AGND1 (Pin 23) with a 100 nF capacitor.
17	DV_{DD}	2.5 V Power Supply for Digital Circuitry and FIR Filter. This pin should be decoupled to the ground plane with a 100 nF capacitor.
22	R_{BIAS}	Bias Current Setting Pin. This pin must be decoupled to the ground plane. For more details, see the Bias Resistor Selection section.
23	AGND1	Power Supply Ground for Analog Circuitry.
20	AGND2	Power Supply Ground for Analog Circuitry.
8	AGND3	Power Supply Ground for Analog Circuitry.
26	REFGND	Reference Ground. Ground connection for the reference voltage.
27	$V_{REF}+$	Reference Input.
1	$V_{IN}A-$	Negative Input to Differential Amplifier.
2	$V_{OUT}A+$	Positive Output from Differential Amplifier.
3	$V_{IN}A+$	Positive Input to Differential Amplifier.
4	$V_{OUT}A-$	Negative Output from Differential Amplifier.
5	$V_{IN}-$	Negative Input to the Modulator.
6	$V_{IN}+$	Positive Input to the Modulator.
9	OVERRANGE	Overrange Pin. This pin outputs a logic high to indicate that the user has applied an analog input that is approaching the limit of the analog input to the modulator.
10	SCO	Serial Clock Out. This clock signal is derived from the internal ICLK signal. The frequency of this clock is equal to ICLK. See the Clocking the AD7764 section for further details.
11	$\overline{FSO}$	Frame Sync Out. This signal frames the serial data output and is 32 SCO periods wide.
12	SDO	Serial Data Out. Data and status are output on this pin during each serial transfer. Each bit is clocked out on an SCO rising edge and is valid on the falling edge. See the AD7764 Interface section for further details.
13	SDI	Serial Data In. The first data bit (MSB) must be valid on the next SCO falling edge after the $\overline{FSI}$ event is latched. Thirty-two bits are required for each write; the first 16-bit word contains the device and register address, and the second word contains the data. See the AD7764 Interface section for further details.

Pin No.	Mnemonic	Description
14	$\overline{\text{FSI}}$	Frame Sync Input. The status of this pin is checked on the falling edge of SCO. If this pin is low, then the first data bit is latched in on the next SCO falling edge. See the AD7764 Interface section for further details.
15	$\overline{\text{SYNC}}$	Synchronization Input. A falling edge on this pin resets the internal filter. This can be used to synchronize multiple devices in a system. See the Synchronization section for further details.
16	$\overline{\text{RESET}}$/ $\overline{\text{PWRDWN}}$	Reset/Power-Down Pin. When a logic low is sensed on this pin, the part is powered down and all internal circuitry is reset.
19	MCLK	Master Clock Input. A low jitter digital clock must be applied to this pin. The output data rate depends on the frequency of this clock. See the Clocking the AD7764 section for more details.
18	DEC_RATE	Decimation Rate. This pin selects one of the three decimation rate modes. When 2.5 V is applied to this pin, a decimation rate of 64× is selected. A decimation rate of 128× is selected by leaving the pin floating. A decimation rate of 256× is selected by setting the pin to ground.

TYPICAL PERFORMANCE CHARACTERISTICS

$AV_{DD}1 = DV_{DD} = 2.5$ V, $AV_{DD}2 = AV_{DD}3 = AV_{DD}4 = 5$ V, $V_{REF}+ = 4.096$ V, MCLK amplitude = 5 V, $T_A = 25°C$. Linearity plots measured to 16-bit accuracy. Input signal reduced to avoid modulator overload and digital clipping; fast Fourier transforms (FFTs) of –0.5 dB tones are generated from 262,144 samples in normal power mode. All other FFTs are generated from 8192 samples.

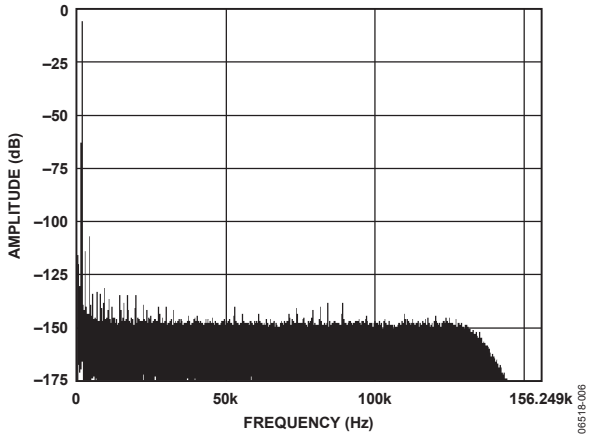

Figure 6. Normal Power Mode, FFT, 1 kHz, –0.5 dB Input Tone, 64× Decimation Rate

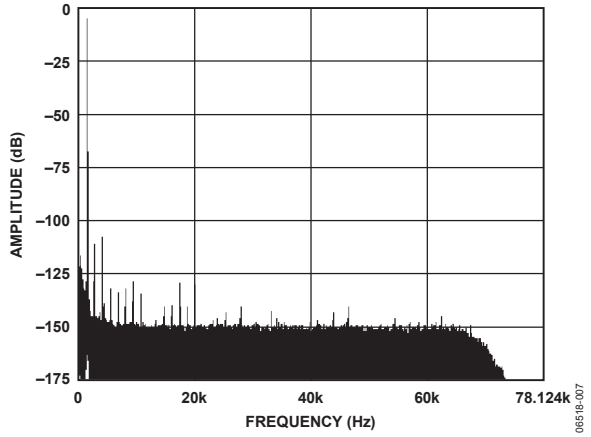

Figure 7. Normal Power Mode, FFT, 1 kHz, –0.5 dB Input Tone, 128× Decimation Rate

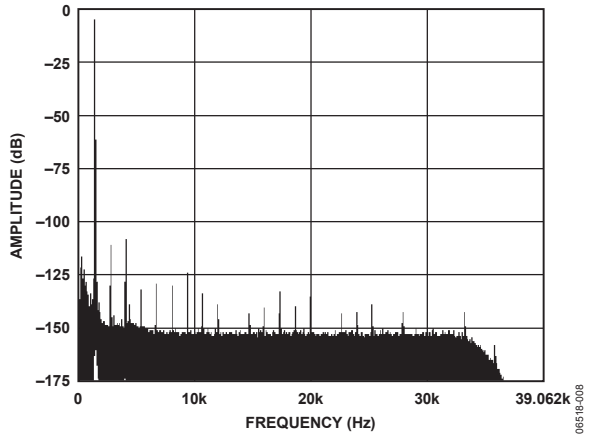

Figure 8. Normal Power Mode, FFT, 1 kHz, –0.5 dB Input Tone, 256× Decimation Rate

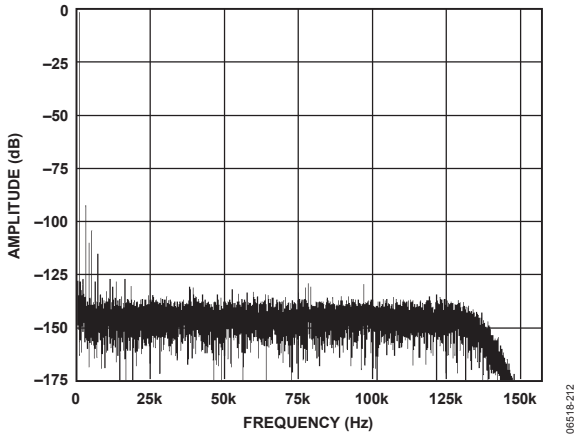

Figure 9. Low Power Mode, FFT, 1 kHz, –0.5 dB Input Tone, 64× Decimation Rate

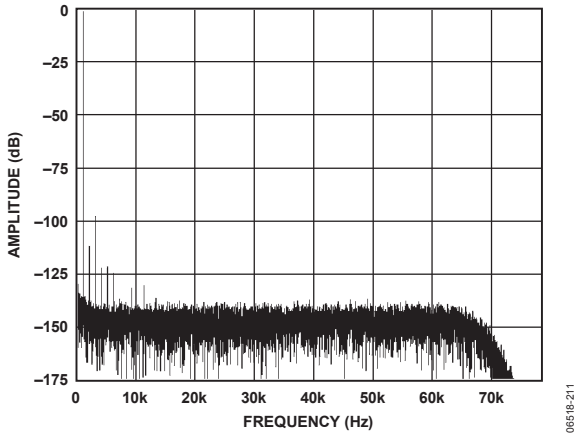

Figure 10. Low Power Mode, FFT, 1 kHz, –0.5 dB Input Tone, 128× Decimation Rate

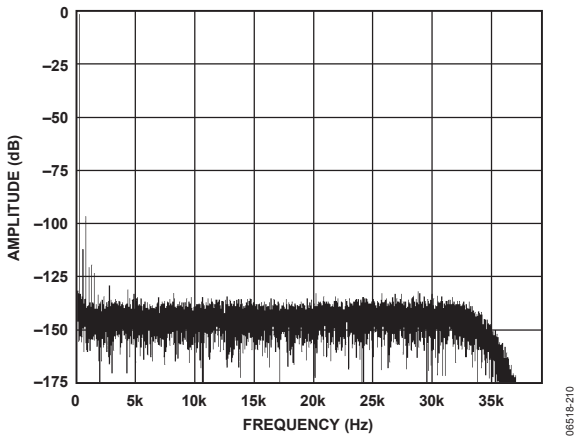

Figure 11. Low Power Mode, FFT, 1 kHz, –0.5 dB Input Tone, 256× Decimation Rate

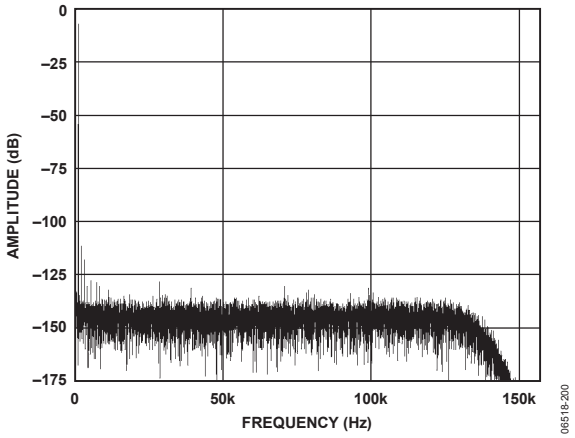

Figure 12. Normal Power Mode, FFT, 1 kHz, −6 dB Input Tone, 64× Decimation Rate

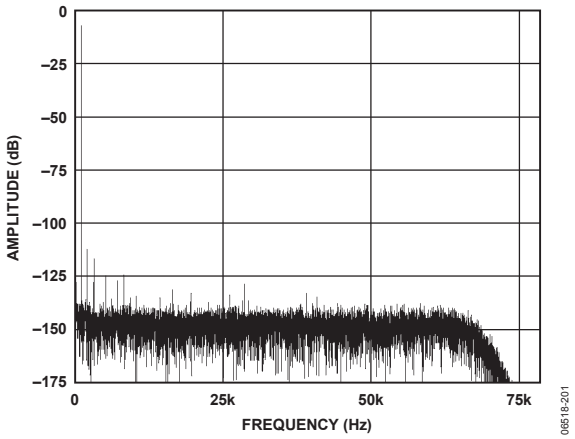

Figure 13. Normal Power Mode, FFT, 1 kHz, −6 dB Input Tone, 128× Decimation Rate

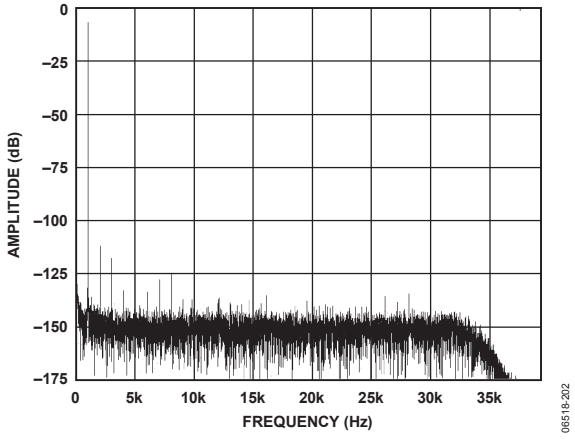

Figure 14. Normal Power Mode, FFT, 1 kHz, −6 dB Input Tone, 256× Decimation Rate

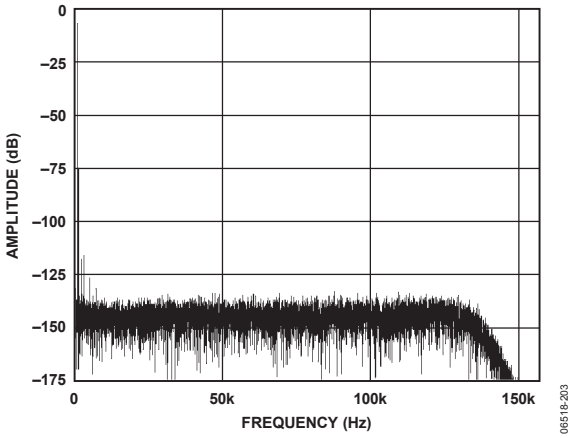

Figure 15. Low Power Mode, FFT, 1 kHz, −6 dB Input Tone, 64× Decimation Rate

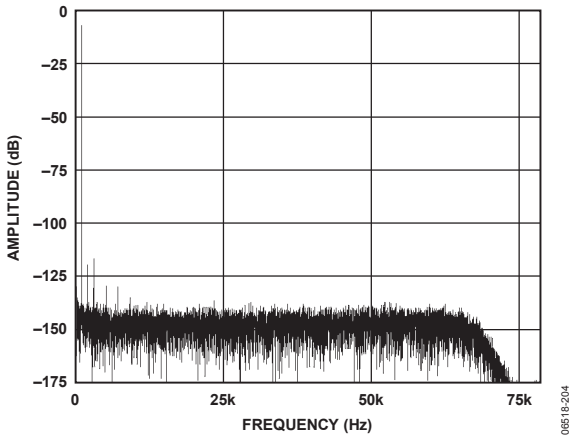

Figure 16. Low Power Mode, FFT, 1 kHz, −6 dB Input Tone, 128× Decimation Rate

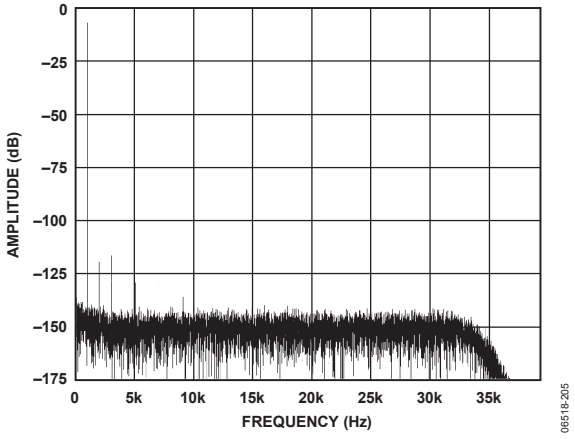

Figure 17. Low Power Mode, FFT, 1 kHz, −6 dB Input Tone, 256× Decimation Rate

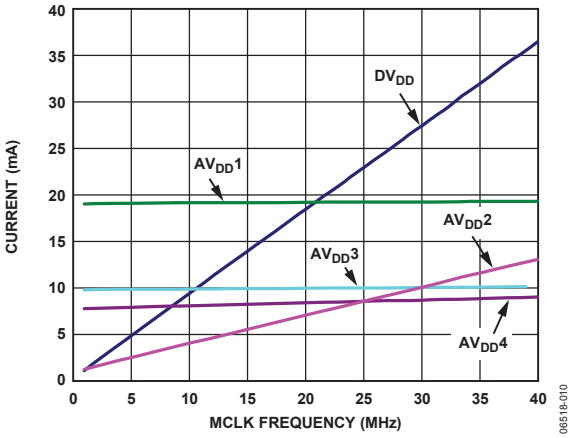

Figure 18. Normal Power Mode, Current Consumption vs. MCLK Frequency, 64× Decimation Rate

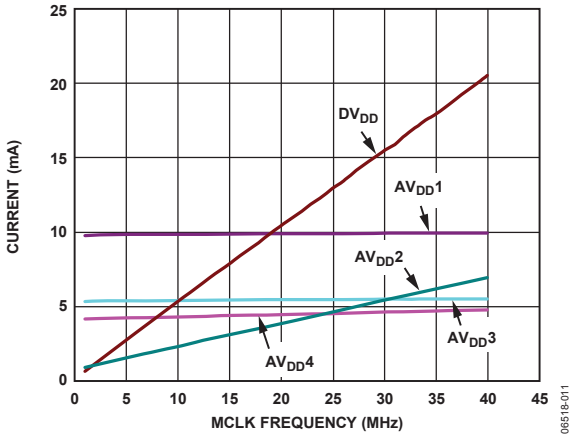

Figure 21. Low Power Mode, Current Consumption vs. MCLK Frequency, 64× Decimation Rate

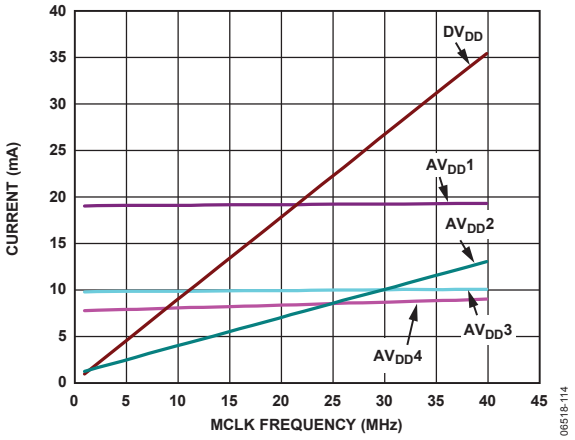

Figure 19. Normal Power Mode, Current Consumption vs. MCLK Frequency, 128× Decimation Rate

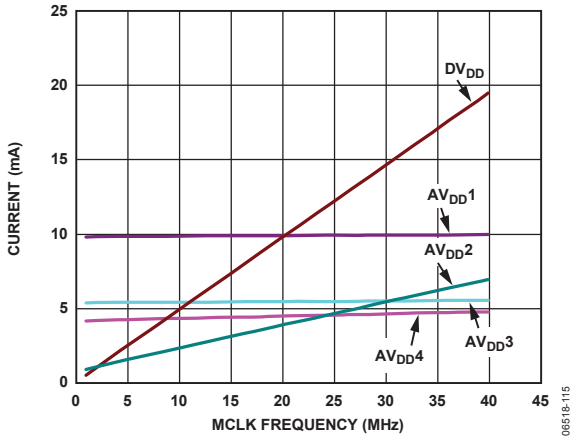

Figure 22. Low Power Mode, Current Consumption vs. MCLK Frequency, 128× Decimation Rate

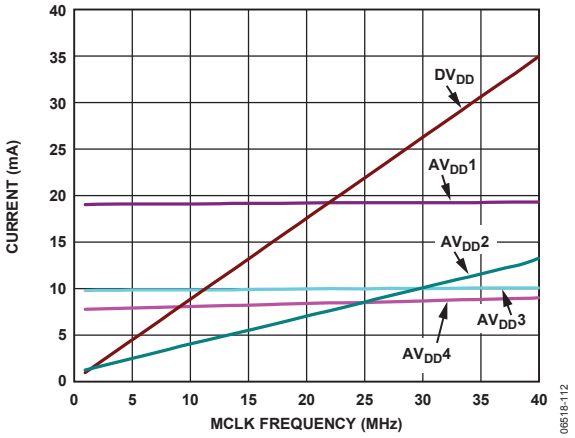

Figure 20. Normal Power Mode, Current Consumption vs. MCLK Frequency, 256× Decimation Rate

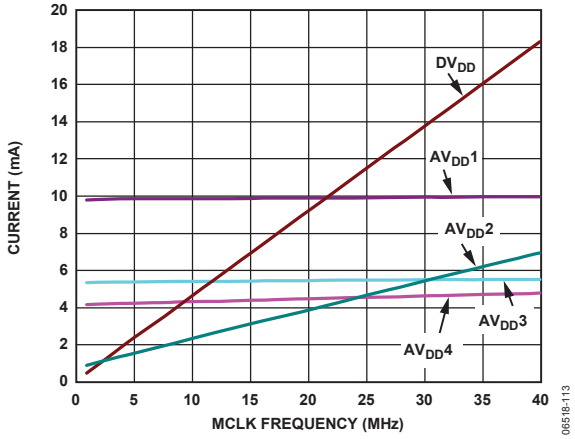

Figure 23. Low Power Mode, Current Consumption vs. MCLK Frequency, 256× Decimation Rate

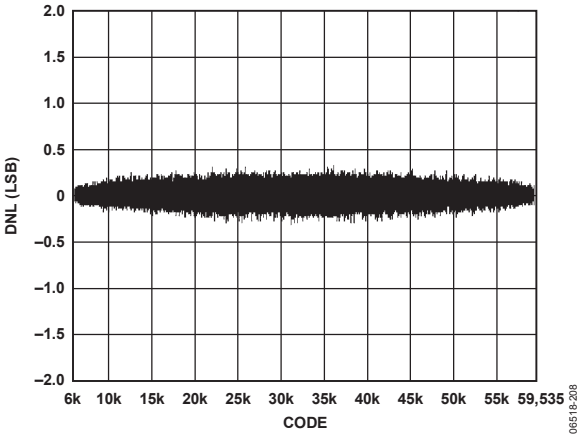

Figure 24. DNL Plot

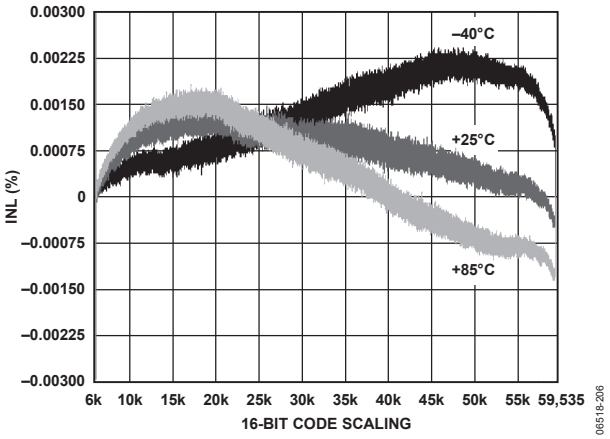

Figure 25. Normal Power Mode INL

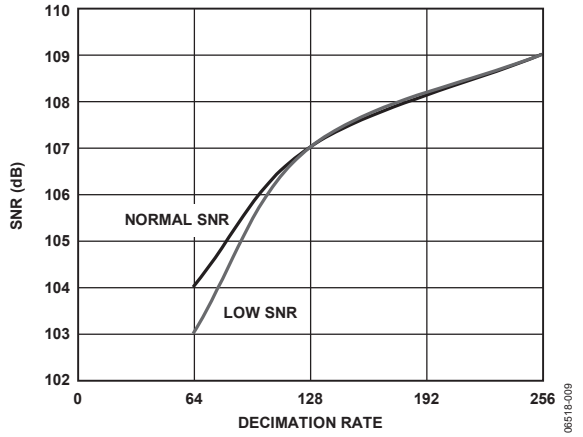

Figure 26. Normal and Low Power Mode, SNR vs. Decimation Rate, 1 kHz, –0.5 dB Input Tone

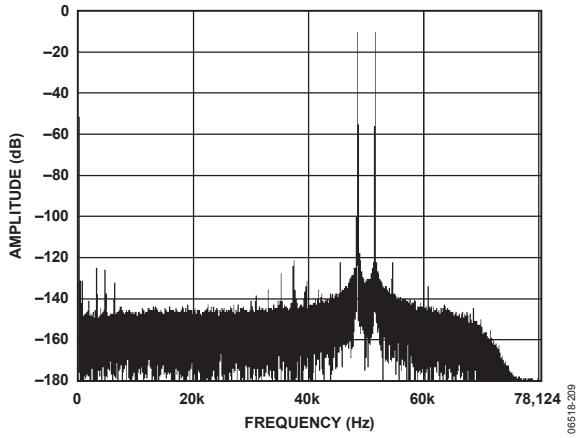

Figure 27. Normal Power Mode, IMD, f_{IN} A = 49.7 kHz, f_{IN} B = 50.3 kHz, 50 kHz Center Frequency, 128× Decimation Rate

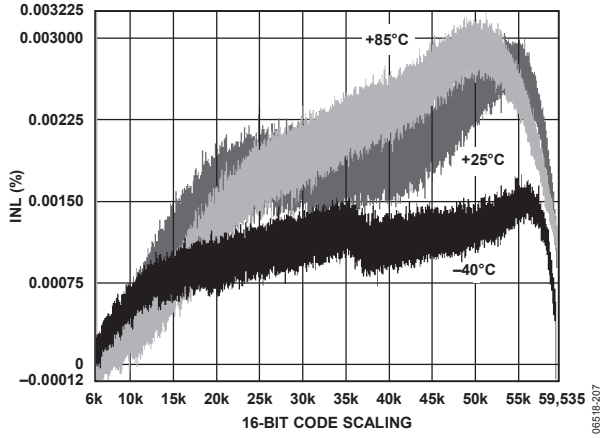

Figure 28. Low Power Mode INL

TERMINOLOGY

Signal-to-Noise Ratio (SNR)
The ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in decibels (dB).

Total Harmonic Distortion (THD)
The ratio of the rms sum of harmonics to the fundamental. For the AD7764, it is defined as

$$THD(\text{dB}) = 20 \log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where:
V_1 is the rms amplitude of the fundamental.
V_2, V_3, V_4, V_5, and V_6 are the rms amplitudes of the second to the sixth harmonics.

Nonharmonic Spurious-Free Dynamic Range (SFDR)
The ratio of the rms signal amplitude to the rms value of the peak spurious spectral component, excluding harmonics.

Dynamic Range
The ratio of the rms value of the full scale to the rms noise measured with the inputs shorted together. The value for dynamic range is expressed in decibels.

Intermodulation Distortion
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities creates distortion products at sum and difference frequencies of mfa ± nfb, where m, n = 0, 1, 2, 3, and so on. Intermodulation distortion terms are those for which neither m nor n is equal to 0. For example, the second-order terms include (fa + fb) and (fa − fb), while the third-order terms include (2fa + fb), (2fa − fb), (fa + 2fb), and (fa − 2fb).

The AD7764 is tested using the CCIF standard, where two input frequencies near the top end of the input bandwidth are used.

In this case, the second-order terms are usually distanced in frequency from the original sine waves, and the third-order terms are usually at a frequency close to the input frequencies. As a result, the second- and third-order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification, where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals expressed in decibels.

Integral Nonlinearity (INL)
The maximum deviation from a straight line passing through the endpoints of the ADC transfer function.

Differential Nonlinearity (DNL)
The difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Zero Error
The difference between the ideal midscale input voltage (when both inputs are shorted together) and the actual voltage producing the midscale output code.

Zero Error Drift
The change in the actual zero error value due to a temperature change of 1°C. It is expressed as a percentage of full scale at room temperature.

Gain Error
The first transition (from 100…000 to 100…001) should occur for an analog voltage 1/2 LSB above the nominal negative full scale. The last transition (from 011…110 to 011…111) should occur for an analog voltage 1 1/2 LSB below the nominal full scale. The gain error is the deviation of the difference between the actual level of the last transition and the actual level of the first transition, from the difference between the ideal levels.

Gain Error Drift
The change in the actual gain error value due to a temperature change of 1°C. It is expressed as a percentage of full scale at room temperature.

THEORY OF OPERATION

The AD7764 features an on-chip fully differential amplifier to feed the Σ-Δ modulator pins, an on-chip reference buffer, and a FIR filter block to perform the required digital filtering of the Σ-Δ modulator output. Using this Σ-Δ conversion technique with the added digital filtering, the analog input is converted to an equivalent digital word.

Σ-Δ MODULATION AND DIGITAL FILTERING

The input waveform applied to the modulator is sampled, and an equivalent digital word is output to the digital filter at a rate equal to ICLK. By employing oversampling, the quantization noise is spread across a wide bandwidth from 0 to f_{ICLK}. This means that the noise energy contained in the signal band of interest is reduced (see Figure 29). To further reduce the quantization noise, a high-order modulator is employed to shape the noise spectrum so that most of the noise energy is shifted out of the signal band (see Figure 30).

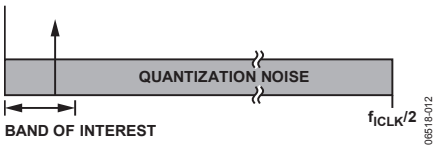

Figure 29. Σ-Δ ADC, Quantization Noise

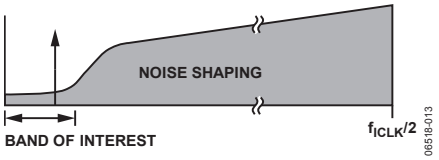

Figure 30. Σ-Δ ADC, Noise Shaping

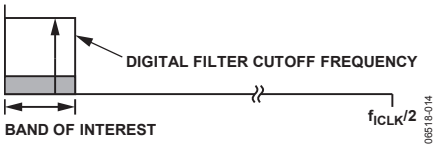

Figure 31. Σ-Δ ADC, Digital Filter Cutoff Frequency

The digital filtering that follows the modulator removes the large out-of-band quantization noise (see Figure 31) while also reducing the data rate from f_{ICLK} at the input of the filter to $f_{ICLK}/64$ or less at the output of the filter, depending on the decimation rate used.

The AD7764 employs three FIR filters in series. By using different combinations of decimation ratios, data can be obtained from the AD7764 at three data rates.

The first filter receives data from the modulator at ICLK MHz where it is decimated 4× to output data at (ICLK/4) MHz. The second filter allows the decimation rate to be chosen from 8× to 32×.

The third filter has a fixed decimation rate of 2×. Table 6 shows some characteristics of the digital filtering where ICLK = MCLK/2. The group delay of the filter is defined to be the delay to the center of the impulse response and is equal to the computation plus the filter delays. The delay until valid data is available (the FILTER-SETTLE status bit is set) is approximately twice the filter delay plus the computation delay. This is listed in terms of MCLK periods in Table 6.

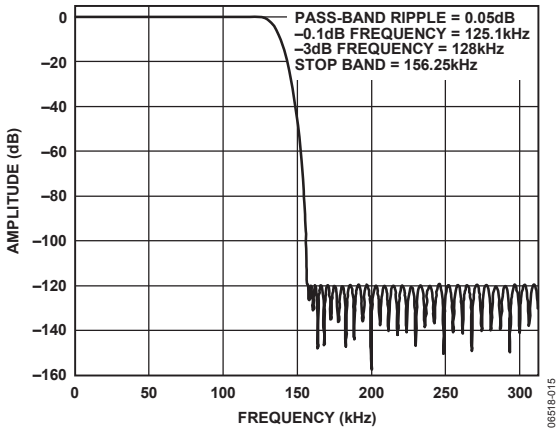

Figure 32. Filter Frequency Response (312.5 kHz ODR)

Table 6. Configuration with Default Filter

ICLK Frequency	Decimation Rate	Data State	Computation Delay	Filter Delay	$\overline{\text{SYNC}}$ to FILTER-SETTLE	Pass-Band Bandwidth	Output Data Rate (ODR)
20 MHz	64×	Fully filtered	2.25 µs	87.6 µs	$7122 \times t_{MCLK}$	125 kHz	312.5 kHz
20 MHz	128×	Fully filtered	3.1 µs	174 µs	$14217 \times t_{MCLK}$	62.5 kHz	156.25 kHz
20 MHz	256×	Fully filtered	4.65 µs	346.8 µs	$27895 \times t_{MCLK}$	31.25 kHz	78.125 kHz
12.288 MHz	64×	Fully filtered	3.66 µs	142.6 µs	$7122 \times t_{MCLK}$	76.8 kHz	192 kHz
12.288 MHz	128×	Fully filtered	5.05 µs	283.2 µs	$14217 \times t_{MCLK}$	38.4 kHz	96 kHz
12.288 MHz	256×	Fully filtered	7.57 µs	564.5 µs	$27895 \times t_{MCLK}$	19.2 kHz	48 kHz

AD7764 ANTIALIAS PROTECTION

The decimation of the AD7764, along with its counterparts in the AD776x family, namely the AD7760, AD7762, AD7763, and AD7765, provides top of the range antialias protection.

The decimation filter of the AD7764 features more than 115 dB of attenuation across the full stop band, which ranges from the Nyquist frequency, namely ODR/2, up to ICLK – ODR/2 (where ODR is the output data rate). Starting the stop band at the Nyquist frequency prevents any signal component above Nyquist (and up to ICLK – ODR/2) from aliasing into the desired signal bandwidth.

Figure 32 shows the frequency response of the decimation filter when the AD7764 is operated with a 40 MHz MCLK in decimate × 128 mode. Note that the first stop-band frequency occurs at Nyquist. The frequency response of the filter scales with both the decimation rate chosen and the MCLK frequency applied. When using low power mode, the modulator sample rate is MCLK/4.

Taking as an example the AD7764 in normal power and in decimate × 128 mode, the first possible alias frequency is at the ICLK frequency minus the pass band of the digital filter (see Figure 33).

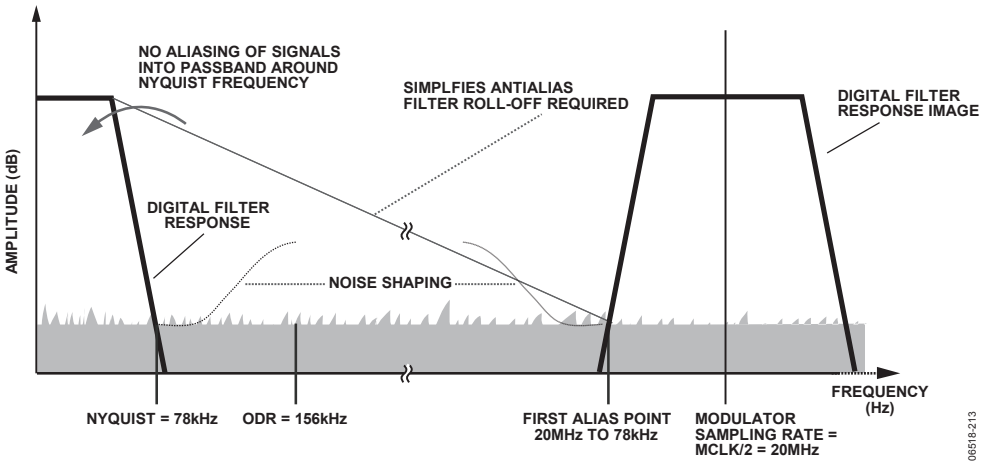

Figure 33. Antialias Example Using the AD7764 in Normal Mode, Decimate × 128 Using MCLK/2 = ICLK = 20 MHz

AD7764 INPUT STRUCTURE

The AD7764 requires a 4.096 V input to the reference pin, $V_{REF}+$, supplied by a high precision reference, such as the ADR444. Because the input to the device's Σ-Δ modulator is fully differential, the effective differential reference range is 8.192 V.

$$V_{REF+(Diff)} = 2 \times 4.096 = 8.192\,V$$

As is inherent in Σ-Δ modulators, only a certain portion of this full reference may be used. With the AD7764, 80% of the full differential reference can be applied to the modulator's differential inputs.

$$Modulator\_Input_{FULLSCALE} = 8.192\,V \times 0.8 = 6.5536\,V$$

This means that a maximum of ±3.2768 V p-p full-scale can be applied to each of the AD7764 modulator inputs (Pin 5 and Pin 6), with the AD7764 being specified with an input −0.5 dB down from full scale (−0.5 dBFS). The AD7764 modulator inputs must have a common-mode input of 2.048 V.

Figure 34 shows the relative scaling between the differential voltages applied to the modulator pins and the respective 24-bit twos complement digital outputs.

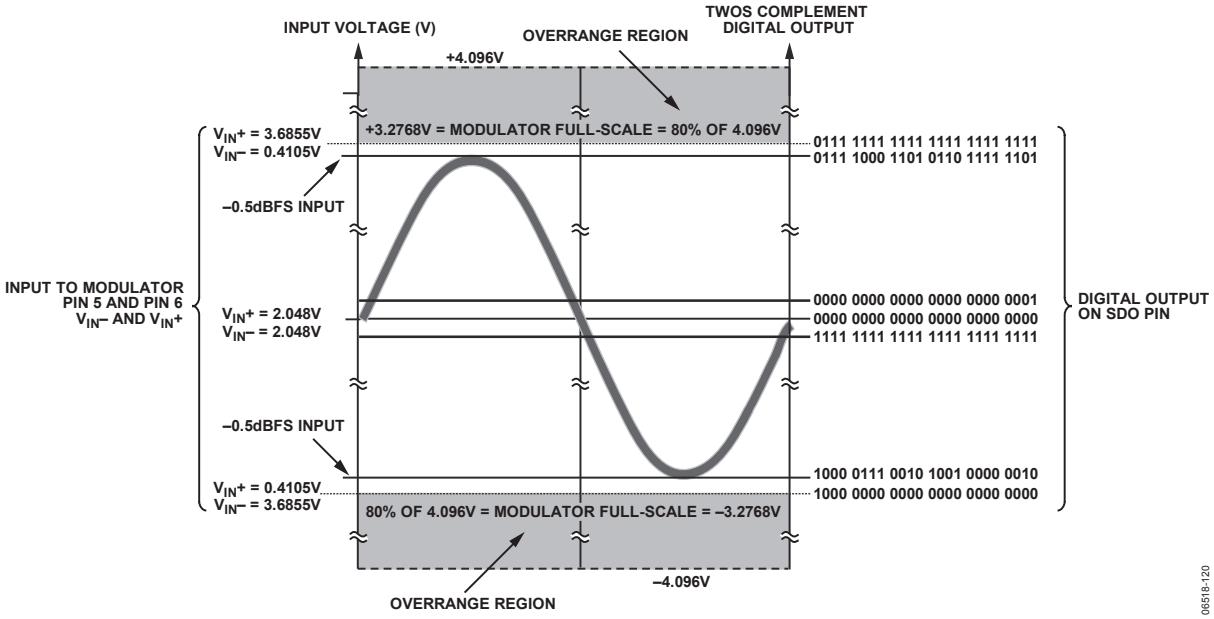

Figure 34. AD7764 Scaling: Modulator Input Voltage vs. Digital Output Code

ON-CHIP DIFFERENTIAL AMPLIFIER

The AD7764 contains an on-board differential amplifier that is recommended to drive the modulator input pins. Pin 1, Pin 2, Pin 3, and Pin 4 on the AD7764 are the differential input and output pins of the amplifier. The external components, R_{IN}, R_{FB}, C_{FB}, C_S, and R_M, are placed around Pin 1 through Pin 6 to create the recommended configuration.

To achieve the specified performance, the differential amplifier should be configured as a first-order antialias filter, as shown in Figure 35, using the component values listed in Table 7. The inputs to the differential amplifier are then routed through the external component network before being applied to the modulator inputs, V_{IN}– and V_{IN}+ (Pin 5 and Pin 6). Using the optimal values in the table as an example yields a 25 dB attenuation at the first alias point of 19.6 MHz.

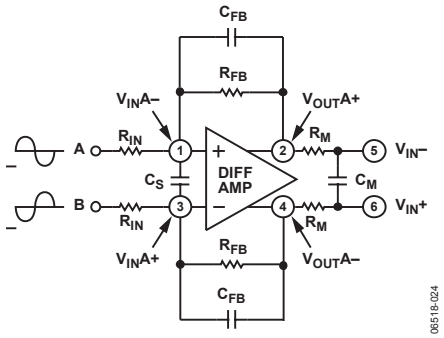

Figure 35. Differential Amplifier Configuration

Table 7. On-Chip Differential Filter Component Values

	R_{IN} (kΩ)	R_{FB} (kΩ)	R_M (Ω)	C_S (pF)	C_{FB} (pF)	C_M (pF)
Optimal	4.75	3.01	43	8.2	47	33
Tolerance Range[1]	2.37 to 5.76	2.4 to 4.87	36 to 47	0 to 10	20 to 100	33 to 56

[1] Values shown are the acceptable tolerances for each component when altered relative to the optimal values used to achieve the stated specifications of the device.

The range of values for each of the components in the differential amplifier configuration is listed in Table 7. When using the differential amplifier to gain the input voltages to the required modulator input range, it is advisable to implement the gain function by changing R_{IN} and leaving R_{FB} as the listed optimal value.

The common-mode input at each of the differential amplifier inputs (Pin V_{IN}A+ and Pin V_{IN}A–) can range from −0.5 V dc to 2.2 V dc. The amplifier has a constant output common-mode voltage of 2.048 V, that is, $V_{REF}/2$, the requisite common mode voltage for the modulator input pins (V_{IN}+ and V_{IN}–).

Figure 36 shows the signal conditioning that occurs using the differential amplifier configuration detailed in Table 7 with a ±2.5 V input signal to the differential amplifier. The amplifier in this example is biased around ground and is scaled to provide ±3.168 V p-p (−0.5 dBFS) on each modulator input with a 2.048 V common mode.

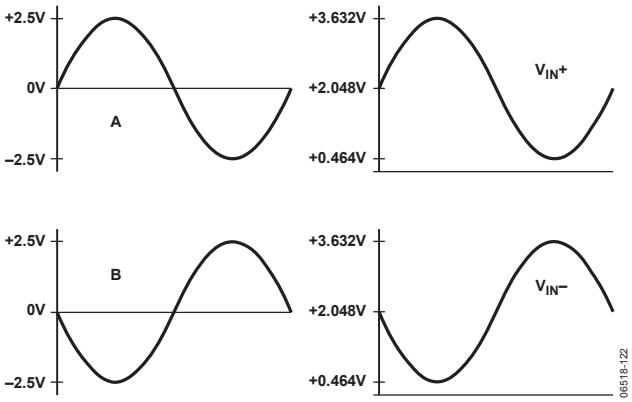

Figure 36. Differential Amplifier Signal Conditioning

To obtain maximum performance from the AD7764, it is advisable to drive the ADC with differential signals. Figure 37 shows how a bipolar, single-ended signal biased around ground can drive the AD7764 with the use of an external op amp, such as the AD8021.

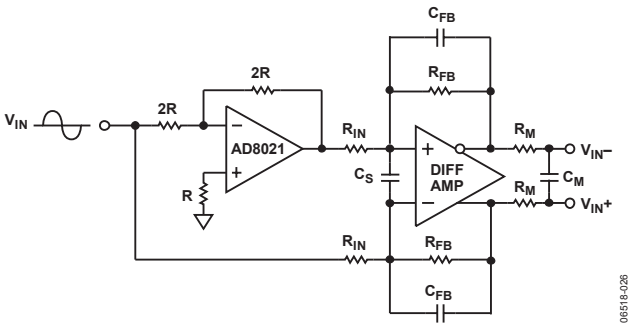

Figure 37. Single-Ended-to-Differential Conversion

MODULATOR INPUT STRUCTURE

The AD7764 employs a double-sampling front end, as shown in Figure 38. For simplicity, only the equivalent input circuitry for V_{IN}+ is shown. The equivalent circuitry for V_{IN}– is the same.

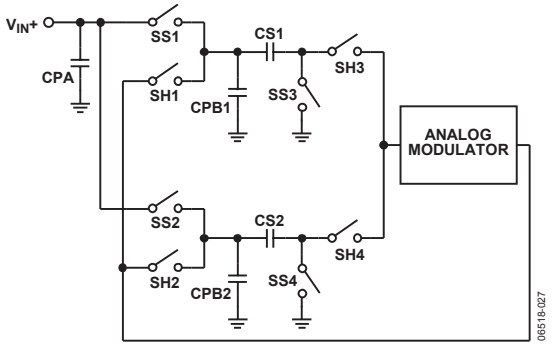

Figure 38. Equivalent Input Circuit

The SS1 and SS3 sampling switches are driven by ICLK, whereas the SS2 and SS4 sampling switches are driven by $\overline{\text{ICLK}}$. When ICLK is high, the analog input voltage is connected to CS1. On the falling edge of ICLK, the SS1 and SS3 switches open, and the analog input is sampled on CS1. Similarly, when ICLK is low, the analog input voltage is connected to CS2. On the rising edge of ICLK, the SS2 and SS4 switches open, and the analog input is sampled on CS2.

The CPA, CPB1, and CPB2 capacitors represent parasitic capacitances that include the junction capacitances associated with the MOS switches.

Table 8. Equivalent Component Values

CS1	CS2	CPA	CPB1/CPB2
13 pF	13 pF	13 pF	5 pF

DRIVING THE MODULATOR INPUTS DIRECTLY

The AD7765 can be configured so that the on-board differential amplifier can be disabled and the modulator can be driven directly using discrete amplifiers. This allows the user to lower the power dissipation.

To power down the on board differential amplifier, the user issues a write to set the AMP OFF bit in the control register to logic high (see Figure 39).

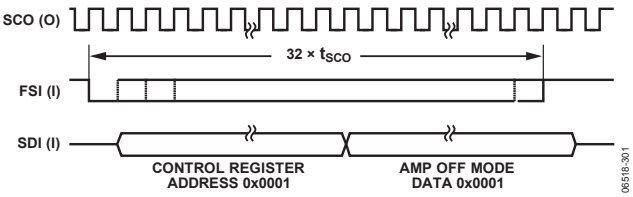

Figure 39. Writing to the AD7764 Control Register Turning Off the On-Board Differential Amplifier

The AD7764 modulator inputs must have a common-mode voltage of 2.048 V and adhere to the amplitudes as described in the AD7764 Input Structure section.

An example of a typical circuit to drive the AD7764 for applications requiring excellent ac and dc performance is shown in Figure 40. Either the AD8606 or AD8656 can be used to drive the AD7764 modulator inputs directly.

Best practice is to short the differential amplifier inputs to ground through the typical input resistors and leave the typical feedback resistors in place.

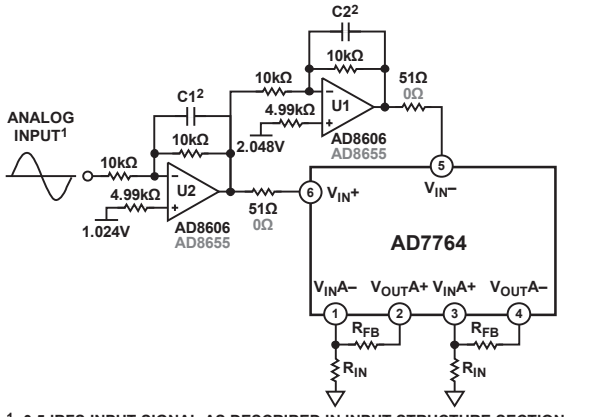

Figure 40. Driving the AD7764 Modulator Inputs Directly from a Single-Ended Source (On-Board Differential Amplifier Powered Down)