



IP PARIS



Data conversion A to D and D to A

Convertisseur Analogique Numérique

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Outline

Introduction

Principle and Quantization Error

Sources of error and evaluation metrics

Main architectures of ADC

Main DAC architectures

Conclusion



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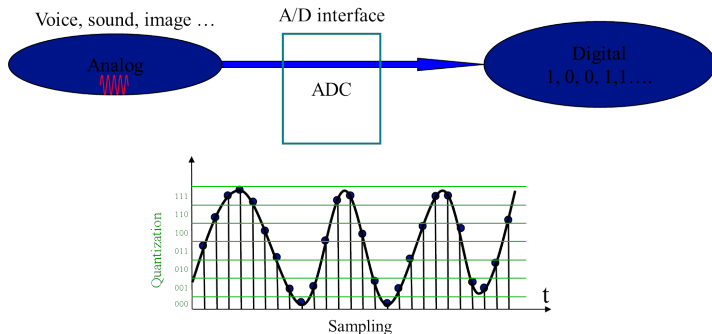
Conclusion

The real world is analog



All communication systems (wired, wireless, fiber-optic), all detection systems (radar, distance sensor ...), and all audio systems are, at some point, analog

Interface



Analog-to-Digital Converter

The Analog-to-Digital Converter is the interface between the real analog world and the digital computing world.

		Amplitude	
		Continuous	Discrete
Time characteristics	Continuous	"Analogue"	"Quantized"
	Discrete	"Sampled"	"Digital"



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Principle

Analog-to-digital conversion requires 2 main steps :

- Discretization in time, or sampling
- Discretization in value, or quantization, which consists in reducing the set of processed values to a set of known values.

Analog-to-Digital Converter

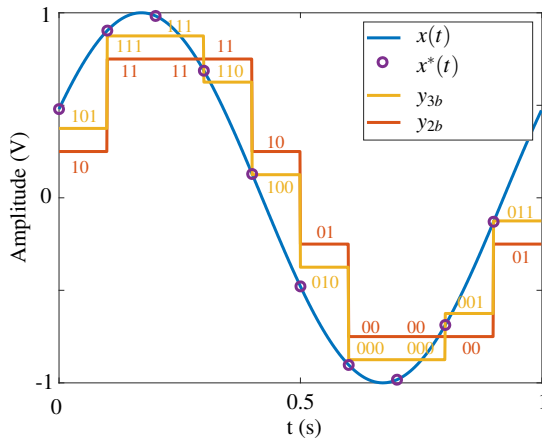
The acronym ADC is used to designate Analog-to-Digital Converters, as well as CAN in French.

Digit-to-Analog Converter

The acronym DAC is used to designate Analog-to-Digital Converters, as well as CNA in French.

Quantization example

$$f_{\text{signal}} = 1 \text{ Hz} \quad A_{\text{Signal}} = 1 \text{ V} \quad f_s = 10 \text{ Hz}$$

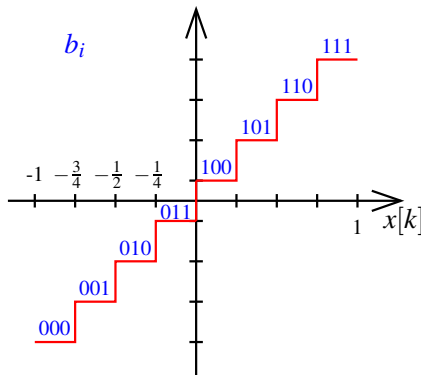


How to perform quantization ?

- Choose a maximum voltage (or any other quantity) V_{max} and a minimum voltage V_{min}
- The difference $V_{max} - V_{min}$ is the full-scale range FS of the ADC
- Divide FS into 2^{nb} equal segments
- The quantization step or quantum q

$$q = \frac{FS}{2^{nb}}$$

- Assign a binary value $b_i[k]$ to each segment



$$nb=3 ; PE=2 \text{ V} ; q=0.25 \text{ V}$$

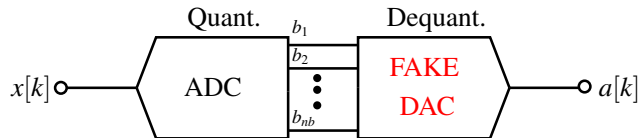
How to evaluate quantization accuracy ?

A quantizer takes a sampled analog signal $x[k]$ as input and outputs a binary bit sequence $b_i[k]$. The 2 quantities are not directly comparable.

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A quantizer takes a sampled analog signal $x[k]$ as input and outputs a binary bit sequence $b_i[k]$. The 2 quantities are not directly comparable.

Solution : “**dequantization**” This consists in adding a fictitious DAC to generate an analog output $a[k]$ corresponding to $b_i[k]$



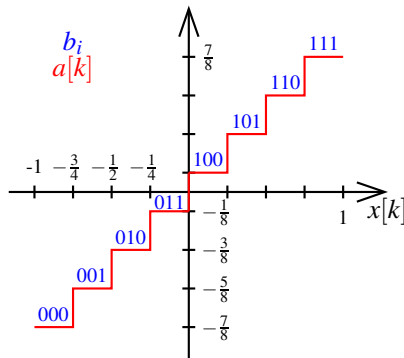
The DAC has the same FS and nb as the ADC

$$\begin{aligned} a[k] &= V_{min} + b_1[k] \frac{FS}{2} + b_2[k] \frac{FS}{4} + \dots \\ &\quad + b_{nb}[k] \frac{FS}{2^{nb}} + \frac{FS}{2^{nb+1}} \\ &= V_{min} + N[k] \frac{FS}{2^{nb}} + \frac{FS}{2^{nb+1}} \\ &= V_{min} + Nq + \underbrace{\frac{q}{2}}_{\text{Added to center the error}} \end{aligned}$$

The quantization error is therefore

$$e[k] = x[k] - a[k]$$

Example

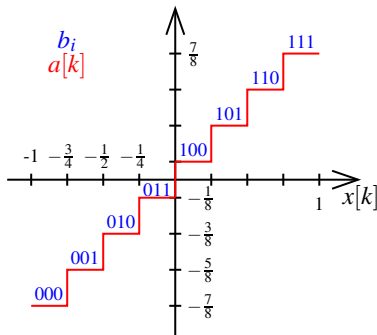


Determine for an analog input $x[k] = -0.53$:

- the digital output $N[k]$
- the binary output $b_i[k]$
- the estimate $a[k]$
- the quantization error $e[k]$

$$nb=3 ; FS=2 \text{ V} ; q=0.25 \text{ V}$$

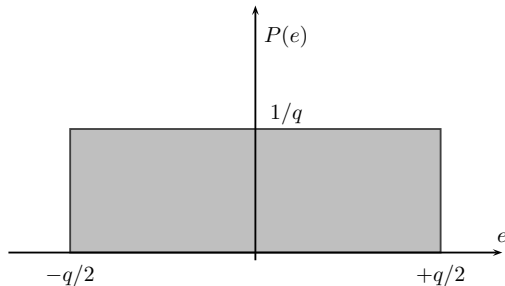
Example



$$nb=3 ; FS=2 \text{ V} ; q=0.25 \text{ V}$$

For $x[k] = -0.53 \text{ V} \Rightarrow N[k] = 1 ; b_i[k] = 001 \quad a[k] = -1 + 0.25 + 0.125 = -0.625 \Rightarrow$
 $e[k] = x[k] - a[k] = 0.095 \text{ V}$

Quantization error



$$\sigma^2 = \frac{1}{q} \int_{-q/2}^{+q/2} e^2 de = \frac{q^2}{12}.$$

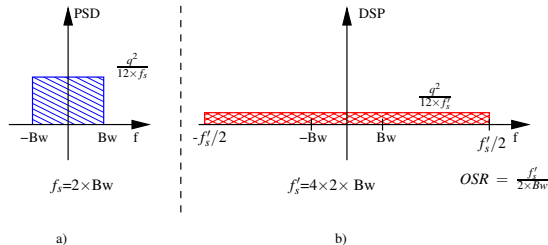
$$SQNR = \frac{\text{Signal Power}}{\text{Noise Power}}$$

$$SQNR = \frac{\int_{-f_s/2}^{+f_s/2} |\text{Signal}(f)|^2 df}{\int_{-f_s/2}^{+f_s/2} PSD_e df}$$

$$\text{If } \text{Signal} = \text{Amp} \sin(2\pi ft), \implies SQNR = \frac{3}{2} \cdot 2^{2nb} \cdot \left(\frac{2 \cdot \text{Amp}}{FS} \right)^2$$

$$\text{In dB : } SQNR_{dB} = 10 \log(SQNR) = 1.76 + 6.02nb + 20 \log \left(\frac{2 \cdot \text{Amp}}{FS} \right)$$

Oversampling



Effect of oversampling

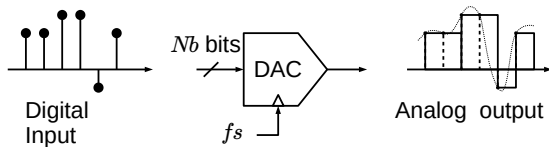
When oversampling, the quantization noise power remains constant but is spread over a wider frequency band

The general expression for SQNR becomes

$$SQNR_{dB} = 10 \log(SQNR) = 1.76 + 6.02nb + 20 \log \left(\frac{2 \cdot Amp}{FS} \right) + 10 \log \left(\frac{f_s}{2 \cdot Bw} \right)$$

What is specific for DAC vs an ADC

- Zero order DAC (rectangular pulse/boxcar function)



- Signal equations :

$$x[n] \longrightarrow x_D(t) = \sum_n x[n] \delta(t - nT_s) \quad (1)$$

$$y_{\text{ZOH}}(t) = \sum_n x[n] h_{\text{ZOH}}(t - nT_s) = x_D * h_{\text{ZOH}}(t) \quad (2)$$

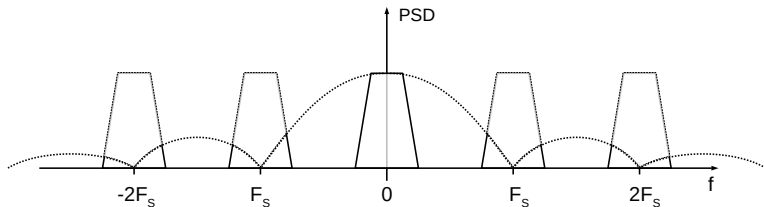
with : $h_{\text{ZOH}}(t) = \text{rect}(t)$

DAC waveforms and ideal reconstruction concept

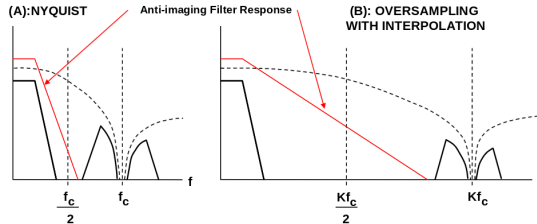
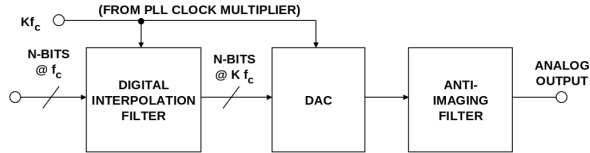
- Basic DAC model : ZOH (rectangular pulse/boxcar function)
- Theoretical spectrum

$$Y_{\text{ZOH}}(f) = X_D(f) \times H_{\text{ZOH}}(f) \quad (4)$$

$$\text{with : } \begin{cases} X_D(f) &= \sum_k X(f - kF_s) \\ H_{\text{ZOH}}(f) &= \text{sinc}(\pi f) \end{cases} \quad (5)$$



Filtering need



A filter is needed at the DAC output to avoid corrupting other bands
The order depends also on the sampling frequency



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Sources of error

The accuracy of data converters (and all electronic systems) is degraded by two main sources :

- Noise, modeled as a random signal added to the useful signal
 - White noise : constant or uniform Power Spectral Density (PSD)
 - Colored noise : non-uniform PSD
- Distortions are errors whose amplitude depends on the input signal
 - Linear distortion, which can be considered as filtering
 - Nonlinear distortion

Noise

■ White noise :

- Thermal noise due to carrier agitation in resistors and transistors
- Quantization noise
- Phase noise causing clock jitter or *jitter*

■ Colored noise

- Flicker noise, *Flicker noise* or $1/f$ noise
- Popcorn noise

Nonlinear distortions

The causes of nonlinear distortions are diverse :

- Saturation
- Inter-symbol interference
- Component mismatches or *mismatch*

Nonlinearities cause :

- A degradation of resolution
- The appearance of new spectral components at multiples of the input frequency.

Main metrics

The Signal-to-Noise Ratio (SNR) is used to evaluate degradation due to noise :

$$SNR_{dB} = 10 \log_{10} \left(\frac{P_{signal}}{P_{Noise}} \right)$$

THD is used to evaluate degradation due to nonlinearities

$$THD_{dB} = -10 \log_{10} \left(\frac{P_{signal}}{P_{Distortion}} \right)$$

SNDR or SINAD (*Signal to Noise and Distortion Ratio*) is used to evaluate degradation due to both

$$SNDR_{dB} = 10 \log_{10} \left(\frac{P_{Signal}}{P_{Noise} + P_{Distortion}} \right)$$

Spectrum example - AD7682

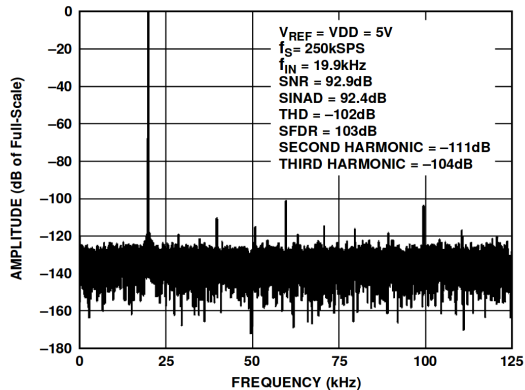


Figure 10. 20 kHz Fast Fourier Transform (FFT), $V_{REF} = V_{DD} = 5V$

SAR ADC AD7682 from Analog Devices

Data converters specifications

- Resolution : SNR, SNDR or SINAD, THD, Dynamic range (DR) , Effective number of bits (ENOB) $ENOB = \frac{SNDR - 1.76}{6.02}$
- Linearity : SFDR, THD, IIP3, IIP2, DNL, INL, ...
- Speed : Data rate ($2 \times Bw$ if no oversampling)



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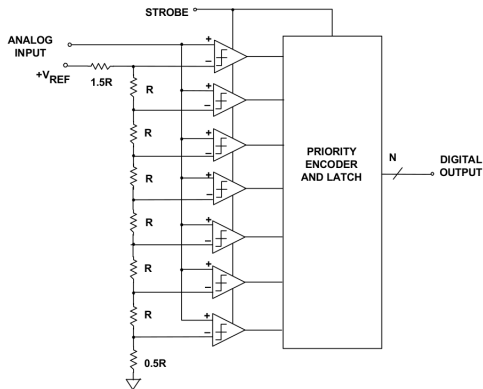
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ADC architectures - Flash



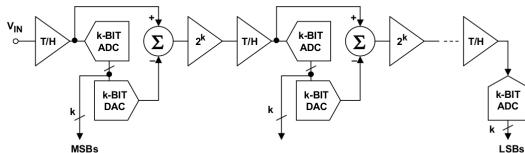
- An N_b -bit Flash ADC requires 2^{N_b-1} comparators (limited resolution)
- The conversion is performed in a single clock cycle (no delay)
- The encoder converts the output thermometer code into a binary code

Accuracy is limited by comparator performance (offset, metastability, hysteresis ...) and resistor matching.

ADC architectures - Pipeline

Pipeline ADC

The conversion is performed using several stages, allowing a higher resolution than Flash with fewer comparators

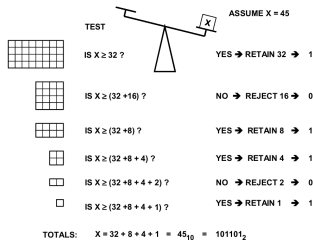
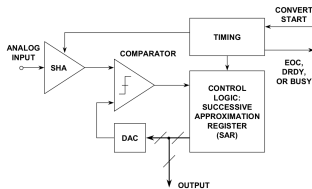


- The first stage performs a coarse quantization which is refined by the following stages
- A Sample&Hold or Track&Hold and amplifiers are required between the stages to amplify the error to the full-scale range

ADC architectures - SAR

SAR ADC

Successive-approximation ADC based on binary search

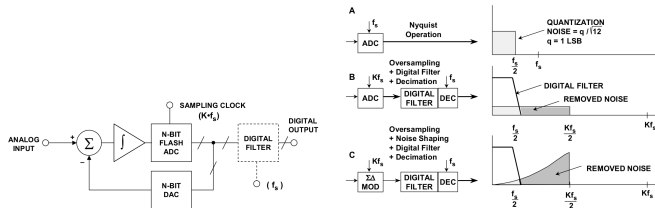


- The resolution is determined by the number of conversion cycles
- The digital-to-analog converter is critical for power consumption and performance in this architecture

ADC architectures - Delta Sigma

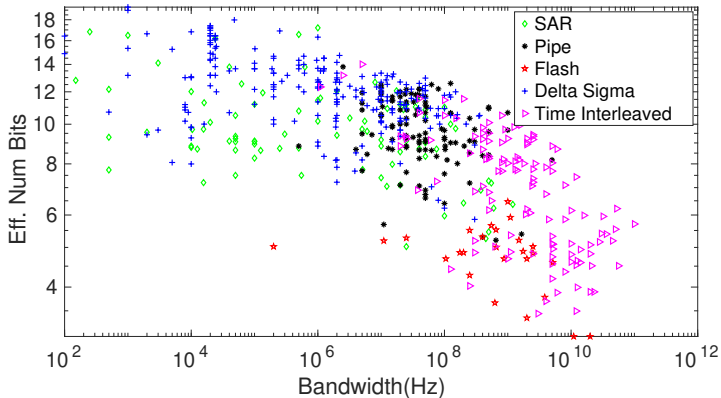
Delta-Sigma ADC

Delta-Sigma ADCs use oversampling and noise shaping to achieve high resolutions.



- Quantization noise is “pushed” out of the useful bandwidth
- A decimation filter is required at the output to return to the Nyquist rate

ADC architectures - Comparison



Resolution vs Bandwidth [Sources : ISSCC and VLSI conferences over 2 decades]

ADC architectures - Comparison

	Flash	Pipeline	SAR	$\Delta\Sigma$
Speed	Very high	high	Average	Low
Resolution	Low	high	high	Very high
Power cons.	Very high	high	Very Low	Low
Area	Very high	high	Low	Average
Drawbacks	Limite resolution. Comparator numbers ↗ exp.	Limited by S/H	Limited by DAC matching	Instability



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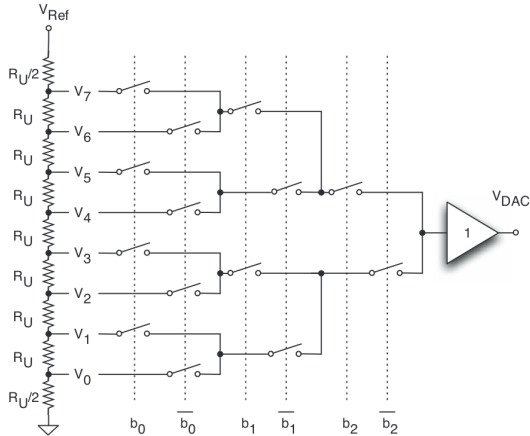
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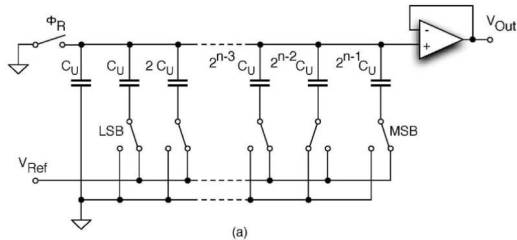
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Resistive DACs



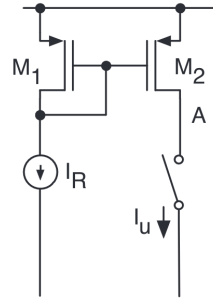
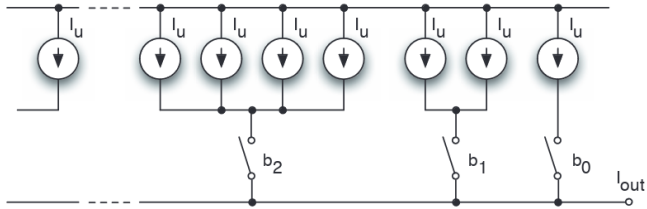
- The output voltage is generated using Resistive ladder. R-2R could be also used
- It has a static power consumption
- It requires an output buffer to drive the load
- Sensitive to Resistor mismatch

Capacitive DACs



- The output voltage is generated using capacitor network
- The power consumption is dynamic.
- Very widely used in ADCs
- Sensitive to capacitor mismatch

Current steering DACs



- The output voltage is created using current steering cells
- Very interesting for high speed applications.
- Dynamic power to drive the switches
- Sensitive to cell mismatch



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- Data converters are key blocks in communication and sensing systems
- Main specifications : speed, FS, resolution, linearity ...
- The choice of the architectures depends on the specifications
- The data converter and the anti-alias/reconstruction filter should be co-designed

Thank you for your attention

Questions ?