ICS905 - Fundamentals in AMS & RF Electronics (FARE)

M2 ICS - Scholar Year 2022-2023(S1)

ICS905 - Exam

Duration 1h30 - Documents and calculator are allowed

Exercises

All exercises are independent.

Direction de la Formation Initiale
Département Communications et Électronique
École Nationale Supérieure des Télécommunications

Exercise 1 - Elements of communication theory and RF systems

The subsections of this exercise (1.1,1.2) can be treated independently

1.1 Signals and systems

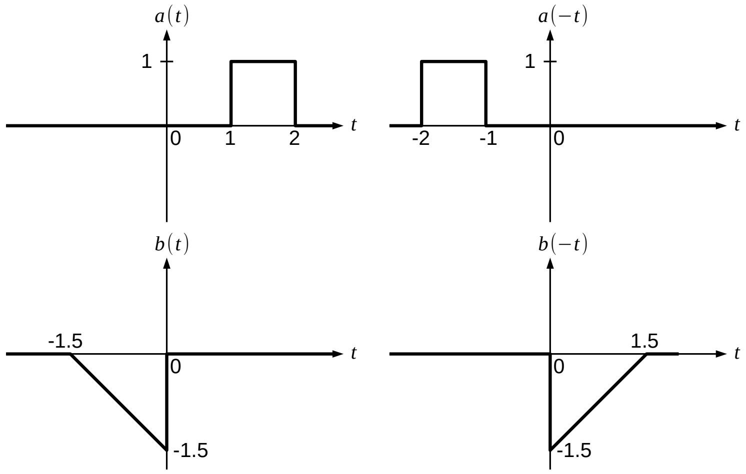


FIGURE 1 – Waveforms of the complex-valued signal $s(t)$

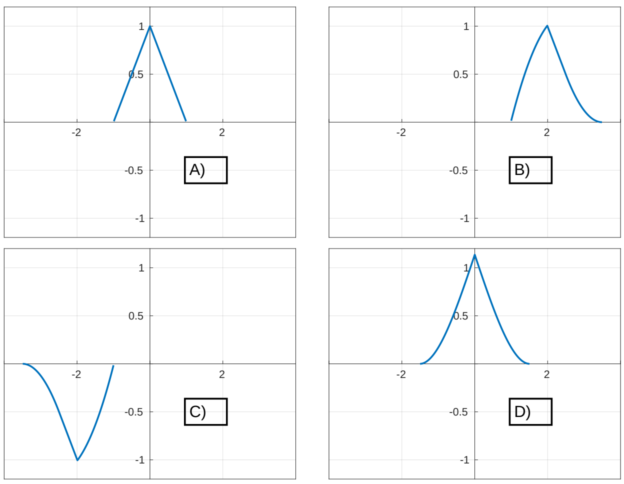
We consider a complex-valued signal $s(t) = a(t) + jb(t)$; the waveforms of $a(t)$ and $b(t)$ are shown in Figure 1. The matched filter is defined as a filter with impulse response $s_{MF}(t) = s^*(-t)$. Note that the Fourier transform is $S_{MF}(f) = S^*(f)$. If the input to the matched filter is $x(t)$, then the output is given by

$$y(t) = (x * s_{MF})(t) = \int_{-\infty}^{\infty} x(u)s_{MF}(t-u)\mathrm{d}u = \int_{-\infty}^{\infty} x(u)s^*(t-u)\mathrm{d}u \tag{1}$$

Question 1.1 Let us consider $y(t) = (s * s_{MF})(t)$ when $s(t)$ is passed through its matched filter ; write $y(t)$ in terms of subcomponents $a(t)$ and $b(t)$ (and convolution products).

Question 1.2 Match the convolution components with the right waveform (for each signal, provide the letter of the associated waveform) :

1. $a(t) * a(-t)$
2. $b(t) * b(-t)$
3. $-a(t) * b(-t)$
4. $b(t) * a(-t)$



Question 1.3 Draw a rough sketch of the magnitude $|y(t)|$. When is the output magnitude the largest ?

1.2 Link budget analysis

You are given an AWGN channel of total bandwidth 3 MHz. The system uses a raised cosine filter with roll-off factor $\alpha = 0.5$.

Question 1.4 What is the value of the baseband symbol rate R_s ?

Question 1.5 Find

- — the achievable bit rate,
- — the E_b/N_0 required for a BER of 10^{-8} using Figure 2 and,
- — the receiver sensitivity (assuming a receiver noise figure of 7 dB)

for the following modulation schemes :

1. QPSK
2. 8-PSK

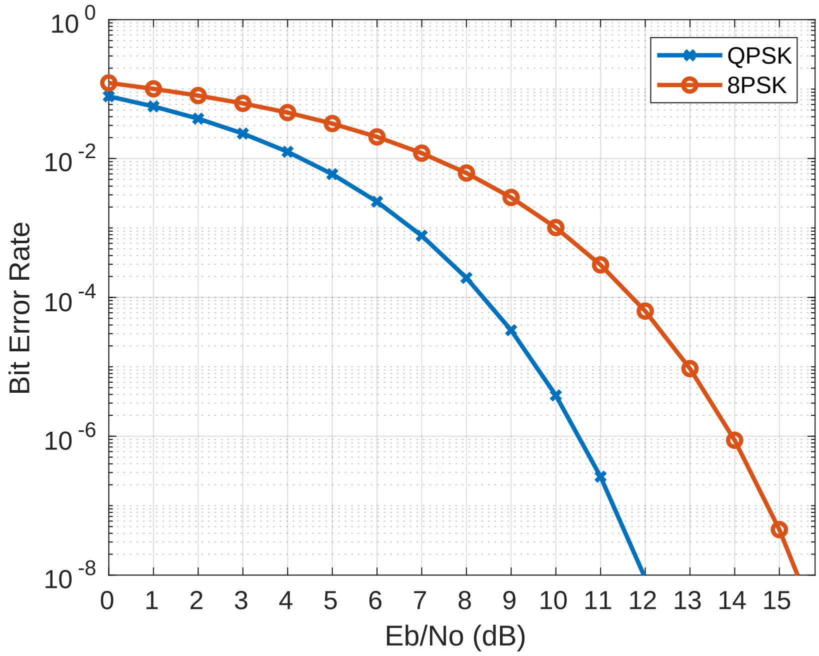


FIGURE 2 – BER for QPSK and 8PSK over AWGN channel

Exercise 2 - Filter for EEG

We would like to design an acquisition system for an electroencephalogram (EEG) application. The considered bandwidth is comprised between 0 and 12 Hz [1]. One major problem for the acquisition is the 50 Hz interferer caused by the electrical network. It needs to be attenuated by at least 60 dB. As for the inband attenuation of the useful signal, it needs to be lower than 3 dB.

Question 2.1 Draw the attenuation template for the needed filter

Question 2.2 Calculate Ω_s and D which are used for order computation. Derive the needed order for a Butterworth approximation.

We decide to use an alternative solution based on the twin-T circuit of figure 3 right).

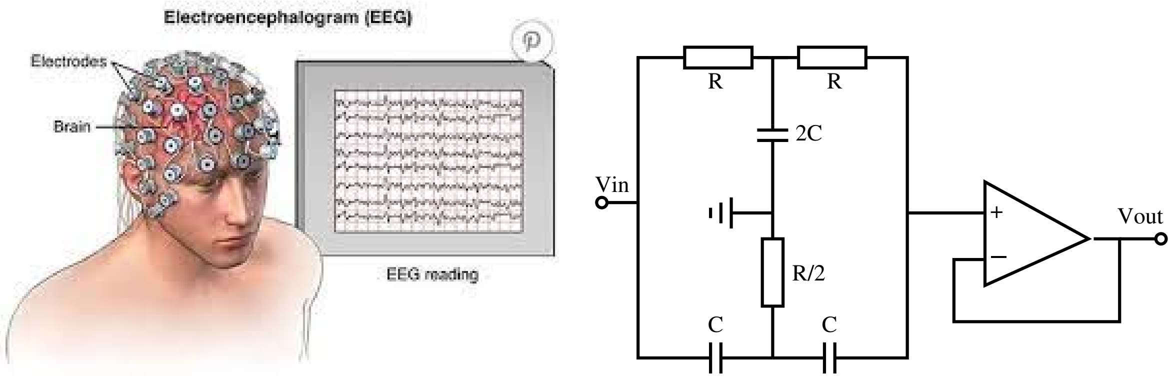


FIGURE 3 – Left) EEG operation. Right) Schematic of the twin-T filter.

Question 2.3 Show that the filter transfer function in Laplace domain is [2] :

$$H(p) = \frac{V_{out}}{V_{in}} = \frac{R^2C^2p^2 + 1}{R^2C^2p^2 + 4RCP + 1}$$

Question 2.4 Plot the bode diagram of the transfer function modulus for $RC = \frac{1}{2\pi 50}$. What is the filter attenuation at 50 Hz ?

Question 2.5 Compare briefly the Butterworth and twin-T solutions.

1. Some of the EEG signals have higher frequencies >30 Hz
2. The operational amplifier could be considered ideal (infinite differential gain and input impedance).

Exercise 3 - Power amplification

Question 3.1 For a power amplifier, what is the ACPR ?

Question 3.2 Consider the transmitter shown in Fig. 4. Calculate the overall gain and Noise Figure.

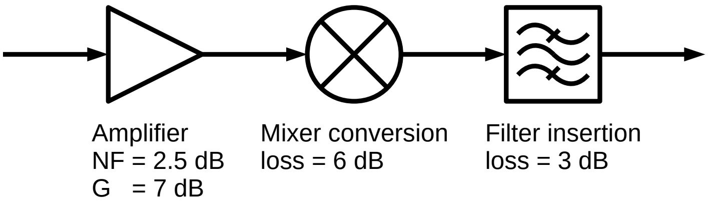


FIGURE 4 – Transmitter specifications

Question 3.3 We need to design a power amplifier with an output power of 12 W, a power gain of 20 dB, a drain efficiency of 25 % and a supply voltage of 30 V at 2 GHz. Calculate the following :

— Required input power : P_{in}
— Required DC drain current : I_{dc}
— Power added efficiency : η_{PAE}

Exercise 4 - ADSL Analog Front End

The ADSL signal is a DTM (Discrete Multi Tones) signal as shown in Fig. 5. It shows a large Peak to RMS ratio.

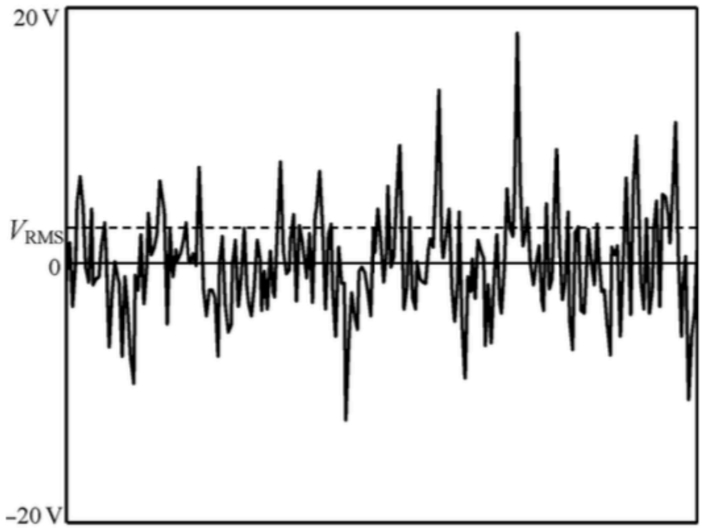


FIGURE 5 – Transmitted DMT time domain signal scaled on the line values

In order to process ADSL signals, we will use a digital receiver meaning that coding and modulation are done in the digital interface by digital signal processing. Still an AFE is mandatory between digital interface and the line as shown in Fig. 6.

A ADSL Analog Front End (AFE) has the following top specifications

— BW = 1.1 MHz
— Supply voltage : ±5 V
— $SNR_{tot} = 80\,\mathrm{dB}$

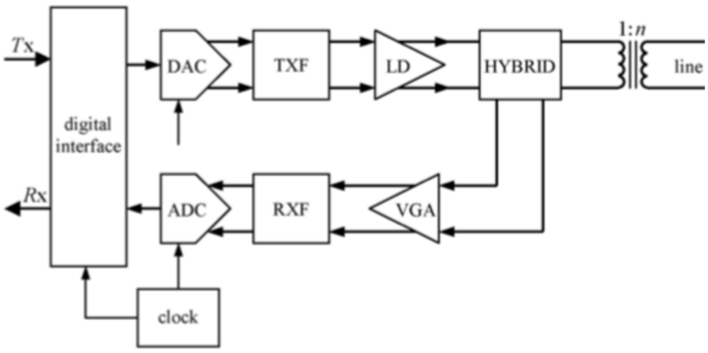


FIGURE 6 – ADSL AFE functional blocks scheme

We have some elements already designed and the purpose of this exercise is to calculate a few specifications for four elements : DAC, ADC, RXF (RX Filter) and VGA (Voltage Gain Amplifier).

Detailed specifications :

— Full Scale (FS) for DAC or ADC can reach at maximum 80 % of the power supply
— The received signal at the input of the VGA is varying in function of the length of the line because of line attenuation :
  — Min rms value : Vrmsmin = 0.1 V
  — Max rms value Vrmsmax = 1 V
  — Peak to RMS ratio = 12 dB
— The partition of the different source of noise in the receiver leads to choose :
  — SNQR = P_S/N_Q where N_Q is the quantization noise power : $SNQR \geq 88\,\mathrm{dB}$
  — P_S is the power of the ADSL signal from the output of the VGA to the input of the digital interface given by $P_S = V_{FSrms}^2/2$
  — $SNR_{VGA} = P_S/N_{VGA}$ where N_{VGA} is the noise power at the output of the VGA introduced by the VGA itself : $SNR_{VGA} \geq 85\,\mathrm{dB}$

Question 4.1 For the DAC and the ADC, calculate the minimum sampling rate, the maximum FS and the minimum resolution.

Question 4.2 Suggest one possible architecture to implement the DAC and justify the interest of this particular architecture.

Question 4.3 Suggest one possible architecture to implement the ADC and justify the interest of this particular architecture.

Question 4.4 What is the role of the RX Filter ? Which type (low pass, high pass, band pass, stop band) ? Which is the specification in term of cut-off frequency ?

The VGA has two main specifications :

— the weak signal at the end of the line should be amplified to the voltage level required at the filter input corresponding to the voltage level requires at the ADC input. It acts as a PGA (Programmable Gain Amplifier)

— The main problem in VGA design is the need to achieve low input noise. It acts as a LNA (Low Noise amplifier)

Question 4.5 Calculate the gain range specification in dB for the VGA.

Question 4.6 Calculate the referred input noise specification V_{RIN} (in V rms) for the VGA such as

$$N_{VGA} = Gain^2 * N_{VGAin} \quad (2)$$

$$N_{VGAin} = V_{RIN}^2/2 \quad (3)$$