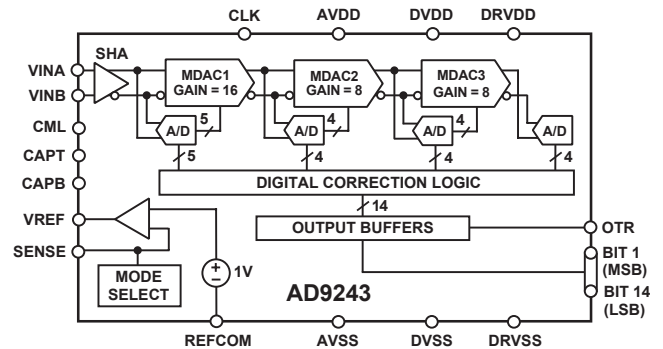


AD9243

FEATURES

Monolithic 14-Bit, 3 MSPS A/D Converter
Low Power Dissipation: 110 mW
Single +5 V Supply
Integral Nonlinearity Error: 2.5 LSB
Differential Nonlinearity Error: 0.6 LSB
Input Referred Noise: 0.36 LSB
Complete: On-Chip Sample-and-Hold Amplifier and Voltage Reference
Signal-to-Noise and Distortion Ratio: 79.0 dB
Spurious-Free Dynamic Range: 91.0 dB
Out-of-Range Indicator
Straight Binary Output Data
44-Lead MQFP

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD9243 is a 3 MSPS, single supply, 14-bit analog-to-digital converter (ADC). It combines a low cost, high speed CMOS process and a novel architecture to achieve the resolution and speed of existing hybrid implementations at a fraction of the power consumption and cost. It is a complete, monolithic ADC with an on-chip, high performance, low noise sample-and-hold amplifier and programmable voltage reference. An external reference can also be chosen to suit the dc accuracy and temperature drift requirements of the application. The device uses a multistage differential pipelined architecture with digital output error correction logic to guarantee no missing codes over the full operating temperature range.

The input of the AD9243 is highly flexible, allowing for easy interfacing to imaging, communications, medical, and data-acquisition systems. A truly differential input structure allows for both single-ended and differential input interfaces of varying input spans. The sample-and-hold amplifier (SHA) is equally suited for both multiplexed systems that switch full-scale voltage levels in successive channels as well as sampling single-channel inputs at frequencies up to and beyond the Nyquist rate. Also, the AD9243 performs well in communication systems employing Direct-IF Down Conversion since the SHA in the differential input mode can achieve excellent dynamic performance *well beyond* its specified Nyquist frequency of 1.5 MHz.

A single clock input is used to control all internal conversion cycles. The digital output data is presented in straight binary output format. An out-of-range (OTR) signal indicates an overflow condition which can be used with the most significant bit to determine low or high overflow.

REV. A

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices.

PRODUCT HIGHLIGHTS

The AD9243 offers a complete single-chip sampling 14-bit, analog-to-digital conversion function in a 44-lead Metric Quad Flatpack.

Low Power and Single Supply

The AD9243 consumes only 110 mW on a single +5 V power supply.

Excellent DC Performance Over Temperature

The AD9243 provides no missing codes, and excellent temperature drift performance over the full operating temperature range.

Excellent AC Performance and Low Noise

The AD9243 provides nearly 13 ENOB performance and has an input referred noise of 0.36 LSB rms.

Flexible Analog Input Range

The versatile onboard sample-and-hold (SHA) can be configured for either single ended or differential inputs of varying input spans.

Flexible Digital Outputs

The digital outputs can be configured to interface with +3 V and +5 V CMOS logic families.

AD9243—SPECIFICATIONS

DC SPECIFICATIONS (AVDD = +5 V, DVDD = +5 V, DRVDD = +5 V, f_{SAMPLE} = 3 MSPS, VREF = 2.5 V, VINB = 2.5 V, T_{MIN} to T_{MAX} unless otherwise noted)

Parameter	AD9243	Units
RESOLUTION	14	Bits min
MAX CONVERSION RATE	3	MHz min
INPUT REFERRED NOISE		
V _{REF} = 1 V	0.9	LSB rms typ
V _{REF} = 2.5 V	0.36	LSB rms typ
ACCURACY		
Integral Nonlinearity (INL)	±2.5	LSB typ
Differential Nonlinearity (DNL)	±0.6	LSB typ
	±1.0	LSB max
INL ¹	±2.5	LSB typ
DNL ¹	±0.7	LSB typ
No Missing Codes	14	Bits Guaranteed
Zero Error (@ +25°C)	0.3	% FSR max
Gain Error (@ +25°C) ²	1.5	% FSR max
Gain Error (@ +25°C) ³	0.75	% FSR max
TEMPERATURE DRIFT		
Zero Error	3.0	ppm/°C typ
Gain Error ²	20.0	ppm/°C typ
Gain Error ³	5.0	ppm/°C typ
POWER SUPPLY REJECTION	0.1	% FSR max
ANALOG INPUT		
Input Span (with V _{REF} = 1.0 V)	2	V p-p min
(with V _{REF} = 2.5 V)	5	V p-p max
Input (VINA or VINB) Range	0	V min
	AVDD	V max
Input Capacitance	16	pF typ
INTERNAL VOLTAGE REFERENCE		
Output Voltage (1 V Mode)	1	Volts typ
Output Voltage Tolerance (1 V Mode)	±14	mV max
Output Voltage (2.5 V Mode)	2.5	Volts typ
Output Voltage Tolerance (2.5 V Mode)	±35	mV max
Load Regulation ⁴	2.0	mV max
REFERENCE INPUT RESISTANCE	5	kΩ typ
POWER SUPPLIES		
Supply Voltages		
AVDD	+5	V (±5% AVDD Operating)
DVDD	+5	V (±5% DVDD Operating)
DRVDD	+5	V (±5% DRVDD Operating)
Supply Current		
IAVDD	23.0	mA max (20 mA typ)
IDRVDD	1.0	mA max (0.5 mA typ)
IDVDD	5.0	mA max (3.5 mA typ)
POWER CONSUMPTION		
	110	mW typ
	145	mW max

NOTES

¹V_{REF} = 1 V.

²Including internal reference.

³Excluding internal reference.

⁴Load regulation with 1 mA load current (in addition to that required by the AD9243).

Specification subject to change without notice.

AC SPECIFICATIONS (AVDD = +5 V, DVDD = +5 V, DRVDD = +5 V, $f_{\text{SAMPLE}} = 3$ MSPS, VREF = 2.5 V, $A_{\text{IN}} = -0.5$ dBFS, AC Coupled/ Differential Input, T_{MIN} to T_{MAX} unless otherwise noted)

Parameter	AD9243	Units
SIGNAL-TO-NOISE AND DISTORTION RATIO (S/N+D) $f_{\text{INPUT}} = 500$ kHz	75.0	dB min
	79.0	dB typ
$f_{\text{INPUT}} = 1.5$ MHz	77.0	dB typ
EFFECTIVE NUMBER OF BITS (ENOB) $f_{\text{INPUT}} = 500$ kHz	12.3	Bits min
	12.8	Bits typ
$f_{\text{INPUT}} = 1.5$ MHz	12.5	Bits typ
SIGNAL-TO-NOISE RATIO (SNR) $f_{\text{INPUT}} = 500$ kHz	76.0	dB min
	80.0	dB typ
$f_{\text{INPUT}} = 1.5$ MHz	79.0	dB typ
TOTAL HARMONIC DISTORTION (THD) $f_{\text{INPUT}} = 500$ kHz	-78.0	dB max
	-87.0	dB typ
$f_{\text{INPUT}} = 1.5$ MHz	-82.0	dB typ
SPURIOUS FREE DYNAMIC RANGE $f_{\text{INPUT}} = 500$ kHz	91.0	dB typ
$f_{\text{INPUT}} = 1.5$ MHz	84.0	dB typ
DYNAMIC PERFORMANCE		
Full Power Bandwidth	40	MHz typ
Small Signal Bandwidth	40	MHz typ
Aperture Delay	1	ns typ
Aperture Jitter	4	ps rms typ
Acquisition to Full-Scale Step (0.0025%)	80	ns typ
Overvoltage Recovery Time	167	ns typ

Specifications subject to change without notice.

DIGITAL SPECIFICATIONS (AVDD = +5 V, DVDD = +5 V, T_{MIN} to T_{MAX} unless otherwise noted)

Parameters	Symbol	AD9243	Units
LOGIC INPUTS			
High Level Input Voltage	V_{IH}	+3.5	V min
Low Level Input Voltage	V_{IL}	+1.0	V max
High Level Input Current ($V_{\text{IN}} = \text{DVDD}$)	I_{IH}	± 10	μA max
Low Level Input Current ($V_{\text{IN}} = 0$ V)	I_{IL}	± 10	μA max
Input Capacitance	C_{IN}	5	pF typ
LOGIC OUTPUTS (with DRVDD = 5 V)			
High Level Output Voltage ($I_{\text{OH}} = 50$ μA)	V_{OH}	+4.5	V min
High Level Output Voltage ($I_{\text{OH}} = 0.5$ mA)	V_{OH}	+2.4	V min
Low Level Output Voltage ($I_{\text{OL}} = 1.6$ mA)	V_{OL}	+0.4	V max
Low Level Output Voltage ($I_{\text{OL}} = 50$ μA)	V_{OL}	+0.1	V max
Output Capacitance	C_{OUT}	5	pF typ
LOGIC OUTPUTS (with DRVDD = 3 V)			
High Level Output Voltage ($I_{\text{OH}} = 50$ μA)	V_{OH}	+2.4	V min
Low Level Output Voltage ($I_{\text{OL}} = 50$ μA)	V_{OL}	+0.7	V max

Specifications subject to change without notice.

AD9243

SWITCHING SPECIFICATIONS (T_{MIN} to T_{MAX} with $AVDD = +5\text{ V}$, $DVDD = +5\text{ V}$, $DRVDD = +5\text{ V}$, $C_L = 20\text{ pF}$)

Parameters	Symbol	AD9243	Units
Clock Period ¹	t_C	333	ns min
CLOCK Pulsewidth High	t_{CH}	150	ns min
CLOCK Pulsewidth Low	t_{CL}	150	ns min
Output Delay	t_{OD}	8	ns min
		13	ns typ
		19	ns max
Pipeline Delay (Latency)		3	Clock Cycles

NOTES

¹The clock period may be extended to 1 ms without degradation in specified performance @ +25°C.

Specifications subject to change without notice.

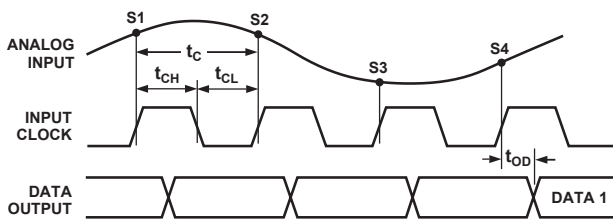


Figure 1. Timing Diagram

ABSOLUTE MAXIMUM RATINGS*

Parameter	With Respect to	Min Max		Units
		Min	Max	
AVDD	AVSS	-0.3	+6.5	V
DVDD	DVSS	-0.3	+6.5	V
AVSS	DVSS	-0.3	+0.3	V
AVDD	DVDD	-6.5	+6.5	V
DRVDD	DRVSS	-0.3	+6.5	V
DRVSS	AVSS	-0.3	+0.3	V
REFCOM	AVSS	-0.3	+0.3	V
CLK	DVSS	-0.3	DVDD + 0.3	V
Digital Outputs	DRVSS	-0.3	DRVDD + 0.3	V
VINA, VINB	AVSS	-0.3	AVDD + 0.3	V
VREF	AVSS	-0.3	AVDD + 0.3	V
SENSE	AVSS	-0.3	AVDD + 0.3	V
CAPB, CAPT	AVSS	-0.3	AVDD + 0.3	V
Junction Temperature			+150	°C
Storage Temperature		-65	+150	°C
Lead Temperature (10 sec)			+300	°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may effect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9243 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

THERMAL CHARACTERISTICS

Thermal Resistance

44-Lead MQFP

$\theta_{JA} = 53.2^\circ\text{C/W}$

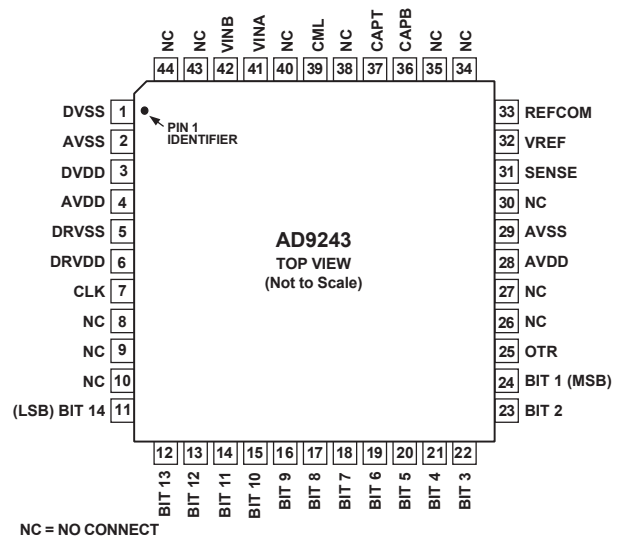
$\theta_{JC} = 19^\circ\text{C/W}$

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD9243AS	-40°C to +85°C	44-Lead MQFP	S-44
AD9243EB	Evaluation Board		

*S = Metric Quad Flatpack.

PIN CONNECTIONS



PIN DESCRIPTION

Pin Number	Name	Description
1	DVSS	Digital Ground
2, 29	AVSS	Analog Ground
3	DVDD	+5 V Digital Supply
4, 28	AVDD	+5 V Analog Supply
5	DRVSS	Digital Output Driver Ground
6	DRVDD	Digital Output Driver Supply
7	CLK	Clock Input Pin
8–10	NC	No Connect
11	BIT 14	Least Significant Data Bit (LSB)
12–23	BIT 13–BIT 2	Data Output Bits
24	BIT 1	Most Significant Data Bit (MSB)
25	OTR	Out of Range
26, 27, 30	NC	No Connect
31	SENSE	Reference Select
32	VREF	Reference I/O
33	REFCOM	Reference Common
34, 35, 38 40, 43, 44	NC	No Connect
36	CAPB	Noise Reduction Pin
37	CAPT	Noise Reduction Pin
39	CML	Common-Mode Level (Midsupply)
41	VINA	Analog Input Pin (+)
42	VINB	Analog Input Pin (–)

DEFINITIONS OF SPECIFICATION

INTEGRAL NONLINEARITY (INL)

INL refers to the deviation of each individual code from a line drawn from “negative full scale” through “positive full scale.” The point used as “negative full scale” occurs 1/2 LSB before the first code transition. “Positive full scale” is defined as a level 1 1/2 LSB beyond the last code transition. The deviation is measured from the middle of each particular code to the true straight line.

DIFFERENTIAL NONLINEARITY (DNL, NO MISSING CODES)

An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. Guaranteed no missing codes to 14-bit resolution indicates that all 16384 codes, respectively, must be present over all operating ranges.

ZERO ERROR

The major carry transition should occur for an analog value 1/2 LSB below VINA = VINB. Zero error is defined as the deviation of the actual transition from that point.

GAIN ERROR

The first code transition should occur at an analog value 1/2 LSB above negative full scale. The last transition should occur at an analog value 1 1/2 LSB below the nominal full scale. Gain error is the deviation of the actual difference between first and last code transitions and the ideal difference between first and last code transitions.

OVERVOLTAGE RECOVERY TIME

Overvoltage recovery time is defined as that amount of time required for the ADC to achieve a specified accuracy after an

overvoltage (50% greater than full-scale range), measured from the time the overvoltage signal reenters the converter’s range.

TEMPERATURE DRIFT

The temperature drift for zero error and gain error specifies the maximum change from the initial (+25°C) value to the value at T_{MIN} or T_{MAX} .

POWER SUPPLY REJECTION

The specification shows the maximum change in full scale from the value with the supply at the minimum limit to the value with the supply at its maximum limit.

APERTURE JITTER

Aperture jitter is the variation in aperture delay for successive samples and is manifested as noise on the input to the A/D.

APERTURE DELAY

Aperture delay is a measure of the sample-and-hold amplifier (SHA) performance and is measured from the rising edge of the clock input to when the input signal is held for conversion.

SIGNAL-TO-NOISE AND DISTORTION (S/N+D, SINAD) RATIO

S/N+D is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for S/N+D is expressed in decibels.

EFFECTIVE NUMBER OF BITS (ENOB)

For a sine wave, SINAD can be expressed in terms of the number of bits. Using the following formula,

$$N = (\text{SINAD} - 1.76)/6.02$$

it is possible to get a measure of performance expressed as N , the effective number of bits.

Thus, effective number of bits for a device for sine wave inputs at a given input frequency can be calculated directly from its measured SINAD.

TOTAL HARMONIC DISTORTION (THD)

THD is the ratio of the rms sum of the first six harmonic components to the rms value of the measured input signal and is expressed as a percentage or in decibels.

SIGNAL-TO-NOISE RATIO (SNR)

SNR is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding the first six harmonics and dc. The value for SNR is expressed in decibels.

SPURIOUS FREE DYNAMIC RANGE (SFDR)

SFDR is the difference in dB between the rms amplitude of the input signal and the peak spurious signal.

TWO-TONE SFDR

The ratio of the rms value of either input tone to the rms value of the peak spurious component. The peak spurious component may or may not be an IMD product. May be reported in dBc (i.e., degrades as signal level is lowered), or in dBFS (always related back to converter full scale).

AD9243

Typical Differential AC Characterization Curves/Plots

($V_{DD} = +5\text{ V}$, $DV_{DD} = +5\text{ V}$, $DRV_{DD} = +5\text{ V}$, $f_{\text{SAMPLE}} = 3.00\text{ MSPS}$, $T_A = +25^\circ\text{C}$, Differential Input)

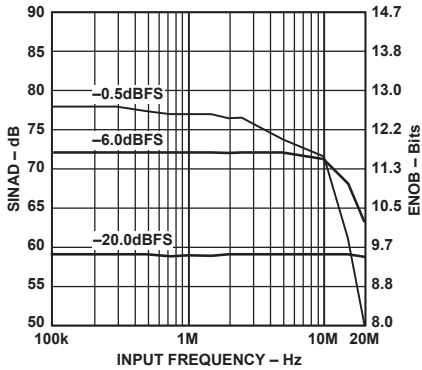


Figure 2. SINAD vs. Input Frequency (Input Span = 5 V, $V_{CM} = 2.5\text{ V}$)

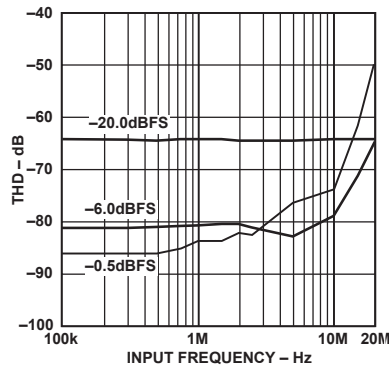


Figure 3. THD vs. Input Frequency (Input Span = 5 V, $V_{CM} = 2.5\text{ V}$)

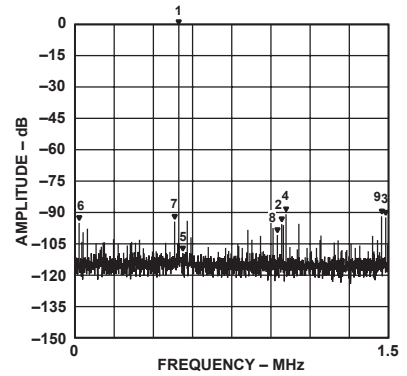


Figure 4. Typical FFT, $f_{IN} = 500\text{ kHz}$ (Input Span = 5 V, $V_{CM} = 2.5\text{ V}$)

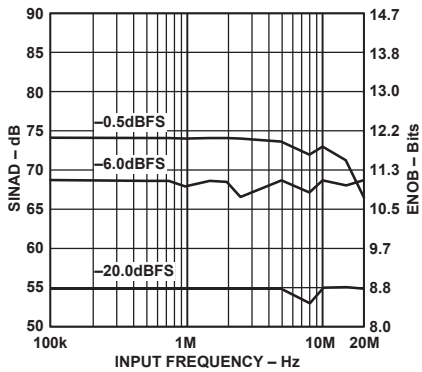


Figure 5. SINAD vs. Input Frequency (Input Span = 2 V, $V_{CM} = 2.5\text{ V}$)

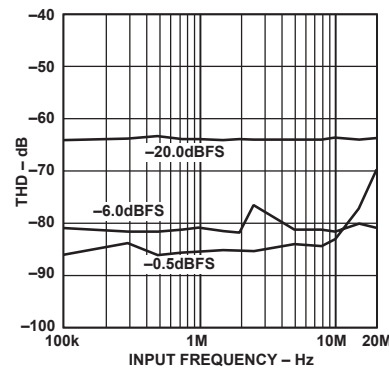


Figure 6. THD vs. Input Frequency (Input Span = 2 V, $V_{CM} = 2.5\text{ V}$)

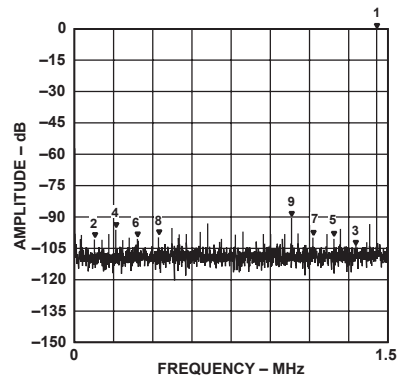


Figure 7. Typical FFT, $f_{IN} = 1.50\text{ MHz}$ (Input Span = 2 V, $V_{CM} = 2.5\text{ V}$)

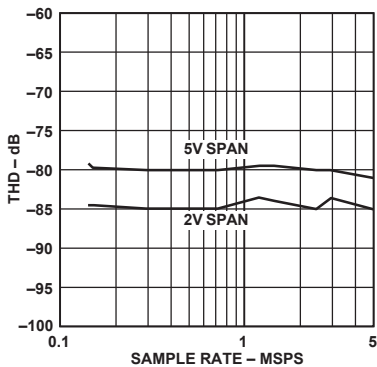


Figure 8. THD vs. Sample Rate ($f_{IN} = 1.5\text{ MHz}$, $A_{IN} = -0.5\text{ dBFS}$, $V_{CM} = 2.5\text{ V}$)

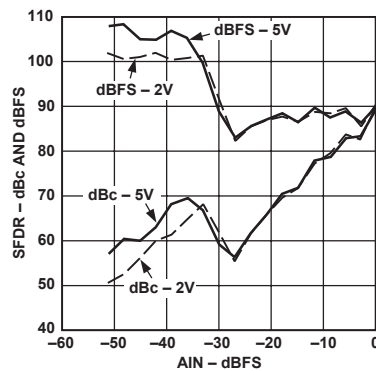


Figure 9. Single Tone SFDR ($f_{IN} = 1.5\text{ MHz}$, $V_{CM} = 2.5\text{ V}$)

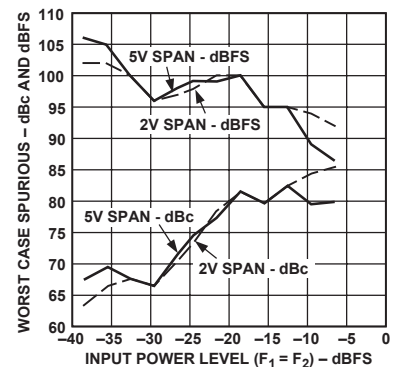


Figure 10. Dual Tone SFDR ($f_1 = 0.95\text{ MHz}$, $f_2 = 1.04\text{ MHz}$, $V_{CM} = 2.5\text{ V}$)

Other Characterization Curves/Plots

(AVDD = +5 V, DVDD = +5 V, DRVDD = +5 V, $f_{SAMPLE} = 3.00$ MSPS, $T_A = +25^\circ\text{C}$, Single-Ended Input)

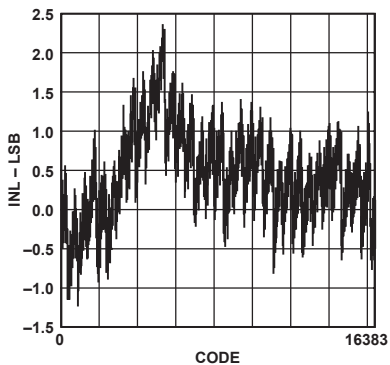


Figure 11. Typical INL (Input Span = 5 V)

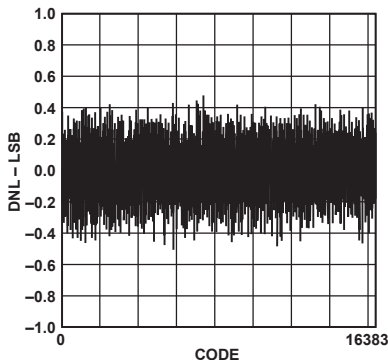


Figure 12. Typical DNL (Input Span = 5 V)

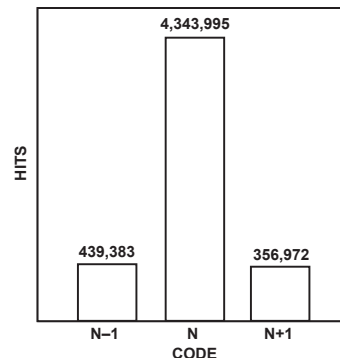


Figure 13. "Grounded-Input" Histogram (Input Span = 5 V)

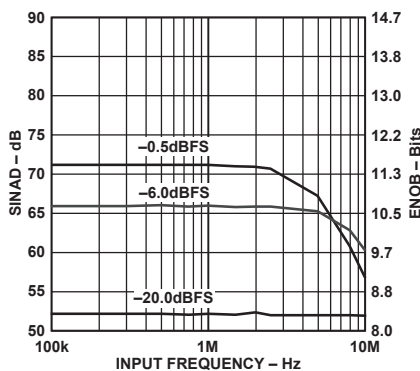


Figure 14. SINAD vs. Input Frequency (Input Span = 2 V, $V_{CM} = 2.5$ V)

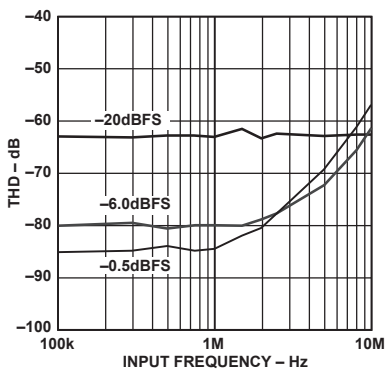


Figure 15. THD vs. Input Frequency (Input Span = 2 V, $V_{CM} = 2.5$ V)

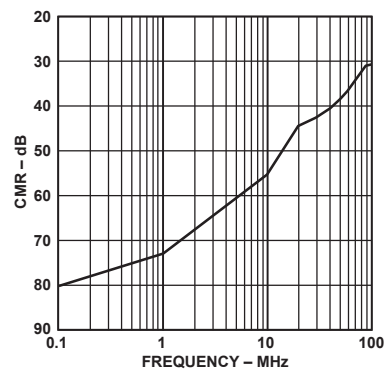


Figure 16. CMR vs. Input Frequency (Input Span = 2 V, $V_{CM} = 2.5$ V)

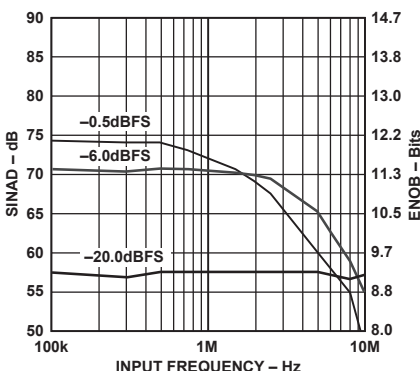


Figure 17. SINAD vs. Input Frequency (Input Span = 5 V, $V_{CM} = 2.5$ V)

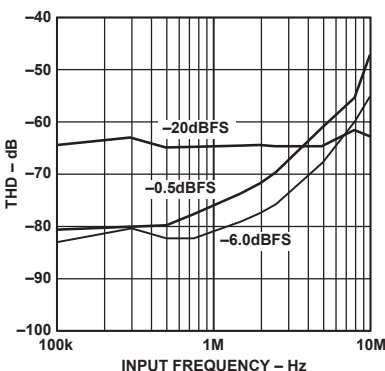


Figure 18. THD vs. Input Frequency (Input Span = 5 V, $V_{CM} = 2.5$ V)

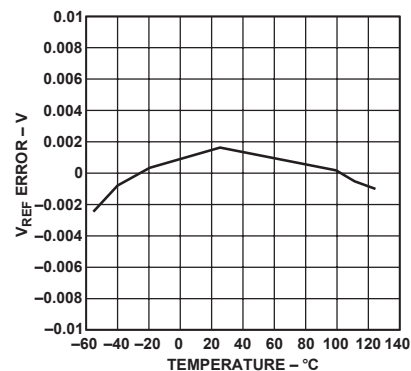


Figure 19. Typical Voltage Reference Error vs. Temperature

AD9243

INTRODUCTION

The AD9243 utilizes a four-stage pipeline architecture with a wideband input sample-and-hold amplifier (SHA) implemented on a cost-effective CMOS process. Each stage of the pipeline, excluding the last stage, consists of a low resolution flash A/D connected to a switched capacitor DAC and interstage residue amplifier (MDAC). The residue amplifier amplifies the difference between the reconstructed DAC output and the flash input for the next stage in the pipeline. One bit of redundancy is used in each of the stages to facilitate digital correction of flash errors. The last stage simply consists of a flash A/D.

The pipeline architecture allows a greater throughput rate at the expense of pipeline delay or latency. This means that while the converter is capable of capturing a new input sample every clock cycle, it actually takes three clock cycles for the conversion to be fully processed and appear at the output. This latency is not a concern in most applications. The digital output, together with the out-of-range indicator (OTR), is latched into an output buffer to drive the output pins. The output drivers can be configured to interface with +5 V or +3.3 V logic families.

The AD9243 uses both edges of the clock in its internal timing circuitry (see Figure 1 and specification page for exact timing requirements). The A/D samples the analog input on the rising edge of the clock input. During the clock low time (between the falling edge and rising edge of the clock), the input SHA is in the sample mode; during the clock high time it is in the hold mode. System disturbances just prior to the rising edge of the clock and/or excessive clock jitter may cause the input SHA to acquire the wrong value, and should be minimized.

ANALOG INPUT AND REFERENCE OVERVIEW

Figure 20, a simplified model of the AD9243, highlights the relationship between the analog inputs, VINA, VINB, and the reference voltage, VREF. Like the voltage applied to the top of the resistor ladder in a flash A/D converter, the value VREF defines the maximum input voltage to the A/D core. The minimum input voltage to the A/D core is automatically defined to be -VREF.

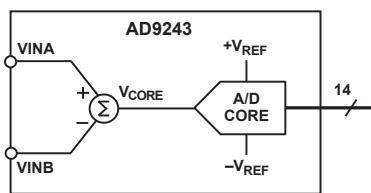


Figure 20. AD9243 Equivalent Functional Input Circuit

The addition of a differential input structure gives the user an additional level of flexibility that is not possible with traditional flash converters. The input stage allows the user to easily configure the inputs for either single-ended operation or differential operation. The A/D's input structure allows the dc offset of the input signal to be varied independently of the input span of the converter. Specifically, the input to the A/D core is the difference of the voltages applied at the VINA and VINB input pins.

Therefore, the equation,

$$V_{CORE} = VINA - VINB \quad (1)$$

defines the output of the differential input stage and provides the input to the A/D core.

The voltage, V_{CORE} , must satisfy the condition,

$$-VREF \leq V_{CORE} \leq VREF \quad (2)$$

where $VREF$ is the voltage at the $VREF$ pin.

While an infinite combination of VINA and VINB inputs exist that satisfy Equation 2, there is an additional limitation placed on the inputs by the power supply voltages of the AD9243. The power supplies bound the valid operating range for VINA and VINB. The condition,

$$AVSS - 0.3 V < VINA < AVDD + 0.3 V \quad (3)$$

$$AVSS - 0.3 V < VINB < AVDD + 0.3 V$$

where $AVSS$ is nominally 0 V and $AVDD$ is nominally +5 V, defines this requirement. Thus, the range of valid inputs for VINA and VINB is any combination that satisfies both Equations 2 and 3.

For additional information showing the relationship between VINA, VINB, VREF and the digital output of the AD9243, see Table IV.

Refer to Table I and Table II for a summary of the various analog input and reference configurations.

ANALOG INPUT OPERATION

Figure 21 shows the equivalent analog input of the AD9243 which consists of a differential sample-and-hold amplifier (SHA). The differential input structure of the SHA is highly flexible, allowing the devices to be easily configured for either a differential or single-ended input. The dc offset, or common-mode voltage, of the input(s) can be set to accommodate either single-supply or dual supply systems. Also, note that the analog inputs, VINA and VINB, are interchangeable with the exception that reversing the inputs to the VINA and VINB pins results in a polarity inversion.

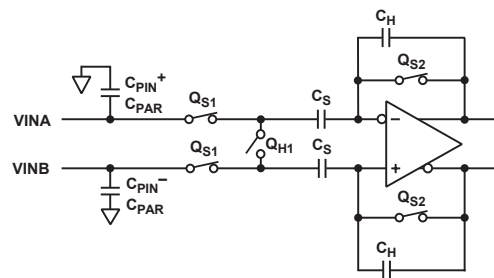


Figure 21. AD9243 Simplified Input Circuit

The input SHA of the AD9243 is optimized to meet the performance requirements for some of the most demanding communication, imaging, and data acquisition applications while maintaining low power dissipation. Figure 22 is a graph of the full-power bandwidth of the AD9243, typically 40 MHz. Note that the small signal bandwidth is the same as the full-power bandwidth. The settling time response to a full-scale stepped input is shown in Figure 23 and is typically 80 ns to 0.0025%. The low input referred noise of 0.36 LSB's rms is displayed via a grounded histogram and is shown in Figure 13.

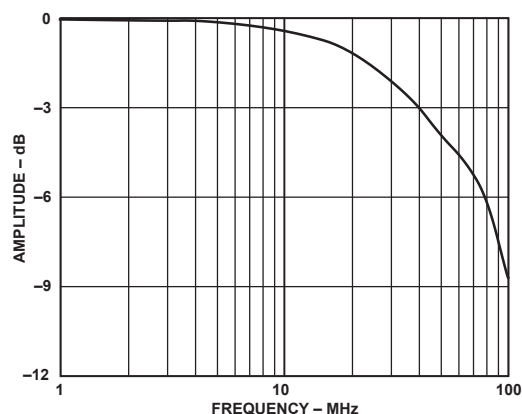


Figure 22. Full-Power Bandwidth

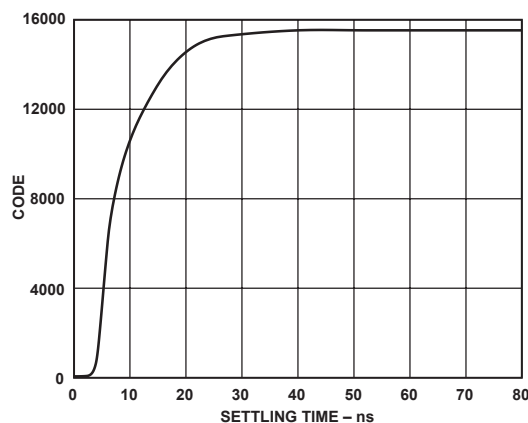


Figure 23. Settling Time

The SHA's optimum *distortion* performance for a differential or single-ended input is achieved under the following two conditions: (1) the common-mode voltage is centered around mid supply (i.e., $AVDD/2$ or approximately 2.5 V) and (2) the input signal voltage span of the SHA is set at its lowest (i.e., 2 V input span). This is due to the sampling switches, Q_{S1} , being CMOS switches whose R_{ON} resistance is very low but has some signal dependency which causes frequency dependent ac distortion while the SHA is in the track mode. The R_{ON} resistance of a CMOS switch is typically lowest at its midsupply but increases symmetrically as the input signal approaches either $AVDD$ or $AVSS$. A lower input signal voltage span centered at midsupply reduces the degree of R_{ON} modulation.

Figure 24 compares the AD9243's THD vs. frequency performance for a 2 V input span with a common-mode voltage of 1 V and 2.5 V. Note the difference in the amount of degrada-

tion in THD performance as the input frequency increases. Similarly, note how the THD performance at lower frequencies becomes less sensitive to the common-mode voltage. As the input frequency approaches dc, the distortion will be dominated by static nonlinearities such as INL and DNL. It is important to note that these dc static nonlinearities are independent of any R_{ON} modulation.

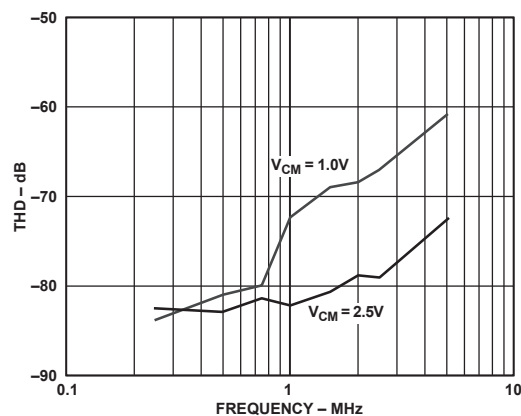


Figure 24. AD9243 THD vs. Frequency for $V_{CM} = 2.5$ V and 1.0 V ($A_{IN} = -0.5$ dB, Input Span = 2.0 V p-p)

Due to the high degree of symmetry within the SHA topology, a significant improvement in distortion performance for differential input signals with frequencies up to and beyond Nyquist can be realized. This inherent symmetry provides excellent cancellation of both common-mode distortion and noise. Also, the required input signal voltage span is reduced by a half which further reduces the degree of R_{ON} modulation and its effects on distortion.

The optimum *noise and dc linearity* performance for either differential or single-ended inputs is achieved with the largest input signal voltage span (i.e., 5 V input span) and matched input impedance for V_{INA} and V_{INB} . Note that only a slight degradation in dc linearity performance exists between the 2 V and 5 V input span as specified in the AD9243 "DC SPECIFICATIONS."

Referring to Figure 21, the differential SHA is implemented using a switched-capacitor topology. Hence, its input impedance and its subsequent effects on the input drive source should be understood to maximize the converter's performance. The combination of the pin capacitance, C_{PIN} , parasitic capacitance C_{PAR} , and the sampling capacitance, C_S , is typically less than 16 pF. When the SHA goes into track mode, the input source must charge or discharge the voltage stored on C_S to the new input voltage. This action of charging and discharging C_S which is approximately 4 pF, averaged over a period of time and for a given sampling frequency, F_S , makes the input impedance appear to have a benign resistive component (i.e., 83 k Ω at $F_S = 3.0$ MSPS). However, if this action is analyzed within a sampling period (i.e., $T = <1/F_S$), the input impedance is dynamic due to the instantaneous requirement of charging and discharging C_S . A series resistor inserted between the input drive source and the SHA input as shown in Figure 25 provides the effective isolation.

AD9243

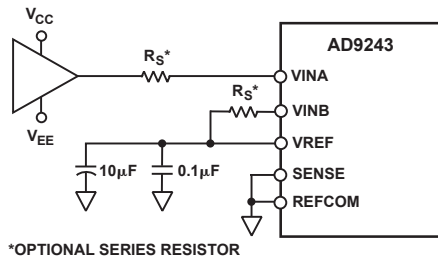


Figure 25. Series Resistor Isolates Switched-Capacitor SHA Input from Op Amp. Matching Resistors Improve SNR Performance

The optimum size of this resistor is dependent on several factors which include the AD9243 sampling rate, the selected op amp, and the particular application. *In most applications, a 30 Ω to 50 Ω resistor is sufficient.* However, some applications may require a larger resistor value to reduce the noise bandwidth or possibly limit the fault current in an overvoltage condition. Other applications may require a larger resistor value as part of an anti-aliasing filter. In any case, since the THD performance is dependent on the series resistance and the above mentioned factors, optimizing this resistor value for a given application is encouraged.

A slight improvement in SNR performance and dc offset performance is achieved by matching the input resistance connected to VINA and VINB. The degree of improvement is dependent on the resistor value and the sampling rate. For series resistor values greater than 100 Ω, the use of a matching resistor is encouraged.

The noise or small-signal bandwidth of the AD9243 is the same as its full-power bandwidth. For noise sensitive applications, the excessive bandwidth may be detrimental and the addition of a series resistor and/or shunt capacitor can help limit the wide-band noise at the A/D's input by forming a low-pass filter. Note, however, that the combination of this series resistance with the equivalent input capacitance of the AD9243 should be evaluated for those time-domain applications that are sensitive to the input signal's absolute settling time. In applications where harmonic distortion is not a primary concern, the series resistance may be selected in combination with the SHA's nominal 16 pF of input capacitance to set the filter's 3 dB cutoff frequency.

A better method of reducing the noise bandwidth, while possibly establishing a real pole for an antialiasing filter, is to add some additional shunt capacitance between the input (i.e., VINA and/or VINB) and analog ground. Since this additional shunt capacitance combines with the equivalent input capacitance of the AD9243, a lower series resistance can be selected to establish the filter's cutoff frequency while not degrading the distortion performance of the device. The shunt capacitance also acts like a charge reservoir, sinking or sourcing the additional charge required by the hold capacitor, C_H , further reducing current transients seen at the op amp's output.

The effect of this increased capacitive load on the op amp driving the AD9243 should be evaluated. To optimize performance when noise is the primary consideration, increase the shunt capacitance as much as the transient response of the input signal will allow. Increasing the capacitance too much may adversely affect the op amp's settling time, frequency response, and distortion performance.

Table I. Analog Input Configuration Summary

Input Connection	Coupling	Input Span (V)	Input Range (V)		Figure #	Comments
			VINA ¹	VINB ¹		
Single-Ended	DC	2	0 to 2	1	32, 33	Best for stepped input response applications, suboptimum THD and noise performance, requires ±5 V op amp.
		$2 \times VREF$	0 to $2 \times VREF$	VREF	32, 33	Same as above but with improved noise performance due to increase in dynamic range. Headroom/settling time requirements of ±5 op amp should be evaluated.
		5	0 to 5	2.5	32, 33	Optimum noise performance, excellent THD performance. Requires op amp with $VCC > +5$ V due to insufficient headroom @ 5 V.
		$2 \times VREF$	$2.5 - VREF$ to $2.5 + VREF$	2.5	39	Optimum THD performance with $VREF = 1$, noise performance improves while THD performance degrades as $VREF$ increases to 2.5 V. Single supply operation (i.e., +5 V) for many op amps.
Single-Ended	AC	2 or $2 \times VREF$	0 to 1 or 0 to $2 \times VREF$	1 or VREF	34	Suboptimum ac performance due to input common-mode level not biased at optimum midsupply level (i.e., 2.5 V).
		5	0 to 5	2.5	34	Optimum noise performance, excellent THD performance.
		$2 \times VREF$	$2.5 - VREF$ to $2.5 + VREF$	2.5	35	Flexible input range, Optimum THD performance with $VREF = 1$. Noise performance improves while THD performance degrades as $VREF$ increases to 2.5 V.
Differential	AC or DC	2	2 to 3	3 to 2	29–31	Optimum full-scale THD and SFDR performance well beyond the A/Ds Nyquist frequency.
		$2 \times VREF$	$2.5 - VREF/2$ to $2.5 + VREF/2$	$2.5 + VREF/2$ to $2.5 - VREF/2$	29–31	Same as 2 V to 3 V input range with the exception that full-scale THD and SFDR performance can be traded off for better noise performance.
		5	1.75 to 3.25	3.25 to 1.75	29–31	Widest dynamic range (i.e., ENOBs) due to Optimum Noise performance.

NOTE

¹VINA and VINB can be interchanged if signal inversion is required.